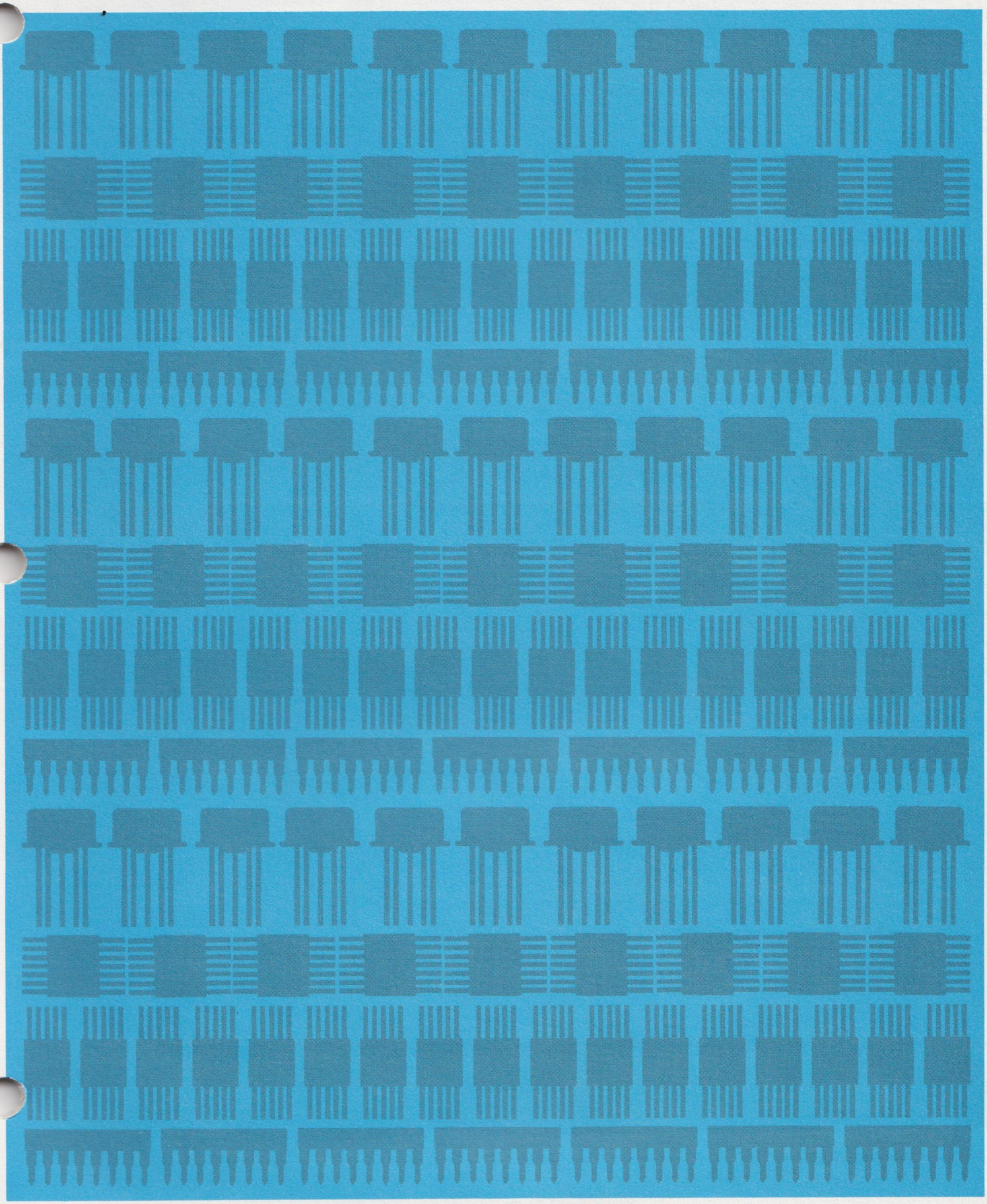
SPRING 1969

CONDENSED CATALOG
SIGNETICS CORPORATION



SIGNETICS PRODUCT LINES

This catalog is designed as a quick reference source on Signetics digital and linear product lines. Its primary purpose is to provide the integrated circuit user with no more than the salient features of each element, including a few typical performance characteristics, logic diagrams (at the back), power supply requirements, packaging, operating temperature range, and primary area of application. Once the reader has found the circuit family or families most likely to meet his needs, he may obtain detailed design data sheets and supporting application data for his selection by returning the enclosed reply card to Signetics Corporation.

APPLICATION DESCRIPTION	DTL	UTILOGIC	UTILOGIC II	LOW POWER TTL DTL	LINEAR	DCL	SECOND SOURCE TTL
ULTRA HIGH RELIABILITY AEROSPACE	RE100			RE400	RE500	R8000	R5400
MILITARY AIRBORNE	SE100			SE400	SE500	S8000	S5400
MILITARY PROTOTYPE GSE	NE100	SU300		NE400	NE500	N8000	N7400
INDUSTRIAL AND COMMERCIAL	SP600	LU300	SP300		NE500	N8000	N7400
FEATURES	LONGEST ESTABLISHED RELIABILITY BEST SPEED/NOISE MARGIN/POWER TRADE OFF	HIGHEST DC NOISE MARGINS HIGH CAPACITANCE DRIVE		LESS THAN 5 mW/GATE DUAL BINARY ACTIVE PULL-UP AND PULL-DOWN	WIDE SELECTION OF GAIN BANDWIDTH PRODUCT	MSI, COMPLEX ARRAYS, INTERFACE GATES, HIGH SPEED, LOW POWER	MSI, COMPLEX ARRAYS HIGH SPEED
SEE PAGE REFERENCED FOR FURTHER INFORMATION	4-5	6		7	11-12-13-14	8-9	10

Index to Signetics Product Codes

Prefix	Designates:
SE, CS, S, R* or RS*	−55°C to +125°C
SU	−20°C to +85°C
N or SP	0°C to +75°C
NE or NS	0°C to +70°C
LU	+10°C to +55°C

*R prefix also designates specially preconditioned high reliability devices.

See SURE Program, pages 15 and 16.

Suffix	Designates:
A	14 lead dual in-line pak
G	10 lead flat pak (TO-91)
K	10 lead TO-5 (TO-100)
J	14 lead flat pak (TO-88)
B	16 lead dual in-line pak
T	8 lead TO-5 (TO-99)
Q	14 lead flat pak
P	24 lead flat pak
R	16 lead flat pak

Which title most closely represents your professional position?

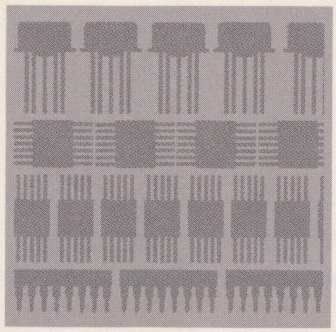
- ☐ Engineering Management
- ☐ Design, Development & Project Engineering
- ☐ All Other Engineering
- ☐ Technician
- ☐ Scientist, Physicist, Chemist, Mathematician
- ☐ Non-Engineering Management
- ☐ Reliability or Evaluation Engineer
- ☐ Purchasing
- ☐ Librarian, Educator

In which area of industry are you employed?

- ☐ Military Electronics
- ☐ Aero/Space
- ☐ Nuclear
- ☐ Test and Measurement Instruments
- ☐ Industrial
- ☐ Consumer
- ☐ Non-electronics industry using electronic products
- ☐ Computer
- ☐ Other

In which type circuits are you more interested?

- ☐ Digital
- ☐ Linear
- ☐ Both



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THE RESPONSE/ABILITY COMPANY

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Which title most closely represents your professional position?

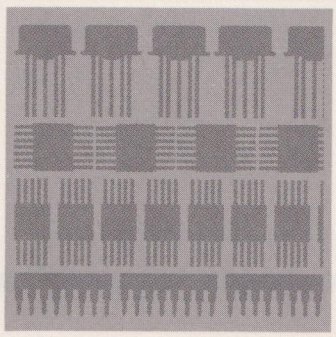
- ☐ Engineering Management
- ☐ Design, Development & Project Engineering
- ☐ All Other Engineering
- ☐ Technician
- ☐ Scientist, Physicist, Chemist, Mathematician
- ☐ Non-Engineering Management
- ☐ Reliability or Evaluation Engineer
- ☐ Purchasing
- ☐ Librarian, Educator

In which area of industry are you employed?

- ☐ Military Electronics
- ☐ Aero/Space
- ☐ Nuclear
- ☐ Test and Measurement Instruments
- ☐ Industrial
- ☐ Consumer
- ☐ Non-electronics industry using electronic products
- ☐ Computer
- ☐ Other

In which type circuits are you more interested?

- ☐ Digital
- ☐ Linear
- ☐ Both



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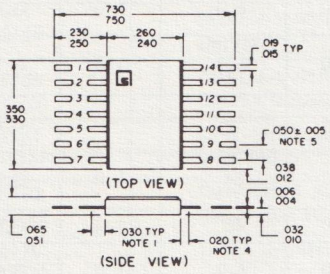
PACKAGES

Outline drawings of the packages used for Signetics products are provided below. Signetics has designed protective carriers for these packages that may be used in testing, handling, shipping, and storage. The mechanical and environmental requirements imposed on these packages are covered in the discussion of the Signetics SURE Program on pages 15 and 16.

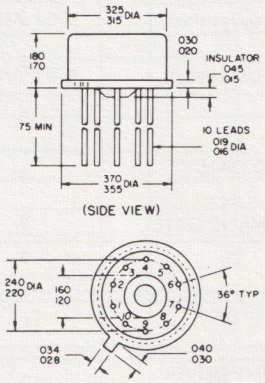
J-PACKAGE (TO-88)

(Modular Glass - Kovar)

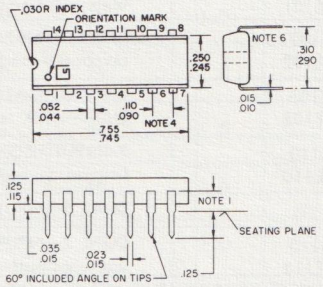


NOTES:
(1) Recommended minimum offset before lead bend.
(2) All leads weldable and solderable.
(3) All dimensions in inches.
(4) Lead spacing dimensions apply to this area only.
(5) Spacing tolerances non-cumulative.
(6) Thermal resistance from junction to still air, $\Theta_{J-A} = 0.3°C/mW$.

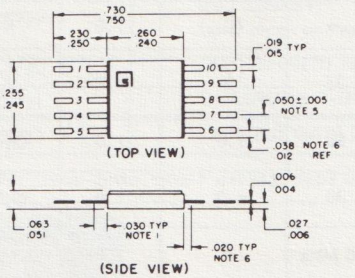
K-PACKAGE (TO-100)



A-PACKAGE (TO-116)

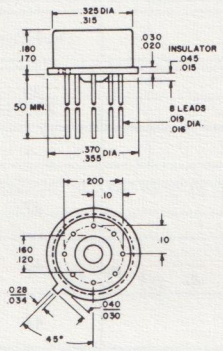


G-PACKAGE (TO-91)



NOTES:
(1) Recommended minimum offset before lead bend.
(2) All leads weldable and solderable.
(3) Pin 1 internally connected to case.
(4) All dimensions in inches.
(5) Tolerances are non-cumulative.
(6) Lead spacing dimensions apply to this area only.
(7) Signetics symbol on flat package locates lead No. 1.
(8) Thermal resistance (both G and K packages) from junction to case, $\Theta_{J-C} = 0.2°C/mW$.

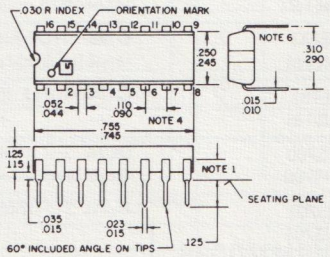
T-PACKAGE (TO-99)



NOTE: Pin 4 internally connected to base.

NOTES:
(for K and T packages)
(1) All dimensions in inches
(2) All leads weldable and solderable

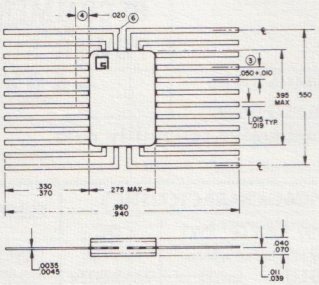
B-PACKAGE



NOTES:
(for A and B packages)
(1) Lead spacing shall be measured within this zone.
(2) Molded Plastic Body.
(3) Kovar Leads.
(4) Lead spacing tolerances are non-cumulative.
(5) Thermal resistance from junction to still air, $\Theta_{J-A} = 0.16°C/mW$.
(6) Leads shown as positioned by Signetics dual in-line package carrier.
(7) All dimensions of plastic package exclude molding-caused flash.

P-PACKAGE

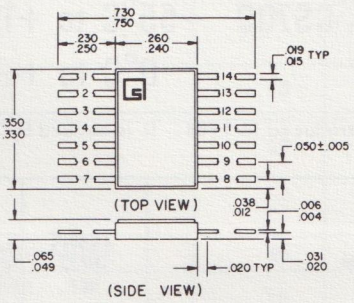
Modular Ceramic (Glass-Seal) - Kovar



NOTES:
1. Lead material: Kovar or Rodar, gold plated.
2. Body material: Kovar or Rodar, top and bottom gold plated with glass center.
3. Tolerances non-cumulative.
4. Lead spacing controlled within this distance, 2 sides.
5. .010 maximum glass climb allowed on leads, 4 sides.
6. Extension denotes lead No. 1 position.

Q-PACKAGE

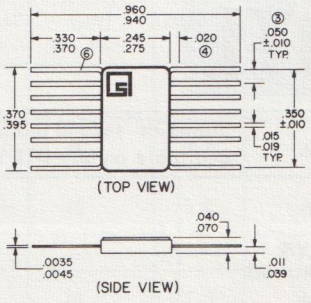
Modular Ceramic (Glass-Seal) - Kovar



NOTES:
(1) Lead material: Kovar or Rodar, gold plated
(2) Body material: Ceramic with glass seals
(3) Lid material: Kovar or Rodar
(4) Tolerances non-cumulative
(5) Lead spacing controlled within this distance, 2 sides
(6) .010 maximum glass climb allowed on leads, 2 sides
(7) Signetics symbol or angle cut identifies lead No. 1

R-PACKAGE

Modular Ceramic (Glass-Seal) - Kovar



NOTES:
(1) Lead material: Kovar or Rodar, gold plated
(2) Body material: Kovar or Rodar, top and bottom gold plated with glass center
(3) Tolerances non-cumulative
(4) Lead spacing controlled within this distance, 2 sides
(5) .010 maximum glass climb allowed on leads, 4 sides
(6) Signetics symbol denotes lead No. 1 position

DTL

SE100, CS700 −55°C to +125°C
NE100, NS700 0°C to + 70°C

RECOMMENDED POWER SUPPLY +4.0V, −2.0V

Signetics first product family, introduced in 1962. This was the industry's first mass-produced integrated circuit DTL family.

TYPE NUMBER	DESCRIPTION	LOGIC DIAG. REF.	FAN-OUT / Function	TYPICAL CHARACTERISTICS			PACKAGE TYPE
				Tpd (ns) AND TOGGLE RATE	AVG. PWR. / Function (mW) 50% Duty	DC NOISE MARGIN (V)	
SE101 NE101	4-INPUT NAND GATE (expansion node and optional pull-up resistor)	1	5	30	6.0	1.0	G,K
SE102 NE102	3-INPUT NAND GATE (expansion node and optional pull-up resistor)	2	5	30	6.0	1.0	G,K
SE105 NE105	6-INPUT GATE EXPANDER (optional 2K resistor)	3	—	—	—	—	G,K
SE110 NE110	3-INPUT HIGH FAN-OUT NAND GATE (expansion node)	5	20	40	34	1.0	G,K
SE113	DUAL 3-INPUT HIGH FAN-OUT NAND GATE	8	15	20	26	1.0	G,K
SE115 NE115	DUAL 2-INPUT NAND GATE (optional pull-up resistor)	9	5	30	6.0	1.0	G,K
SE124 NE124	RS/T BINARY (asynchronous set and reset)	11	8	18 MHz	18	1.0	G,K
SE150 NE150	2-INPUT CLOCK/CAPACITIVE LINE DRIVER	13	20	40	36	1.0	G,K
SE157 NE157	DUAL 3-INPUT CLOCK/CAPACITVE LINE DRIVER	16	15	20	26	1.0	K
SE160 NE160	ONE-SHOT MULTIVIBRATOR (expansion node)	17	4	—	32	1.0	G,K
SE161 NE161	ONE-SHOT MULTIVIBRATOR (enable/disable input)	18	5	—	40	1.0	K
SE181 NE181	QUADRUPLE INVERTER	22	5	25	12	1.0	K
CS700 NS700	DUAL 3-2 INPUT NAND GATE (bare output collector)	4	5	30	6.0	1.0	G,K
CS701 NS701	DUAL 3-2-INPUT NAND GATE	42	4	30	9.0	1.0	G,K
CS704	RS/T BINARY (split clock and asychronous set)	43	8	18 MHz	18	1.0	G,K
CS705	DUAL 3-INPUT AND GATE	44	—	3	4	—	G,K
CS709	DUAL 3-INPUT GATE EXPANDER	45	—	—	—	—	G,K
CS715	DUAL 2-INPUT CLOCK/CAPACITIVE LINE DRIVER (expansion node)	46	15	22	26	1.0	K
CS716 NS716	DUAL 2-INPUT HIGH FAN-OUT NAND GATE (expansion node)	47	15	22	26	1.0	K

DTL

SE100, CS700 −55°C to +125°C
NE100 0°C to + 70°C

RECOMMENDED POWER SUPPLY +4.0V

Signetics second product family, introduced in 1964. It is backed by the most comprehensive reliability data available on any DTL family.

TYPE NUMBER	DESCRIPTION	LOGIC DIAG. REF.	FAN-OUT / Function	TYPICAL CHARACTERISTICS			PACKAGE TYPE Note 1:
				Tpd (ns) AND TOGGLE RATE	AVG. PWR. / Function (mW) 50% Duty	DC NOISE MARGIN (V)	
SE106 NE106	DUAL 5-INPUT GATE EXPANDER	41	—	—	—	—	J*
SE111	DUAL 4-INPUT HIGH FAN-OUT NAND GATE	6	19	20	26	1.0	J

TYPE NUMBER	DESCRIPTION	LOGIC DIAG. REF.	FAN-OUT Function	TYPICAL CHARACTERISTICS			PACKAGE TYPE Note 1
				Tpd (ns) AND TOGGLE RATE	AVG. PWR. Function (mV) 50% Duty	DC NOISE MARGIN (V)	
SE112 NE112	DUAL 3-INPUT HIGH FAN-OUT NAND GATE (expansion node and optional pull-up resistor)	7	19	20	26	1.0	J*
SE116 NE116	DUAL 4-INPUT NAND GATE (expansion node)	10	6	25	12	1.0	J*
SE124 NE124	RS/T BINARY (asynchronous set and reset)	11	7	18 MHz	18	1.0	J*
SE125 NE125	J-K BINARY (multi J/K and inverting J/K)	12	8	12 MHz	60	1.0	J*
SE155	DUAL 4-INPUT CLOCK/CAPACITIVE LINE DRIVER	14	19	20	26	1.0	J
SE156 NE156	DUAL 4-INPUT CLOCK/CAPACITIVE LINE DRIVER (expansion node)	15	19	20	26	1.0	J*
SE161 NE161	ONE-SHOT MULTIVIBRATOR (gate input)	18	4	—	51	1.0	J*
SE162 NE162	ONE-SHOT MULTIVIBRATOR (delay from 80 ns to 2 seconds)	19	12	35	65	1.0	J
SE170 NE170	TRIPLE 3-INPUT NAND GATE	20	6	25	12	1.0	J*
SE180 NE180	QUADRUPLE 2-INPUT NAND GATE	21	6	25	12	1.0	J*
CS720	QUADRUPLE 2-INPUT NAND GATE (bare output collector)	38	6	25	10.5	1.0	J
CS721	TRIPLE 3-INPUT NAND GATE (bare output collector)	36	6	25	10.5	1.0	J
CS727	TRIPLE 2-INPUT NAND GATE (expansion node)	48	6	25	12	1.0	J
CS729	RS/T BINARY (split clock and asynchronous set and reset)	39	7	18 MHz	18	1.0	J
CS730	DUAL 5-INPUT NAND GATE	49	6	25	12	1.0	J
CS731	QUADRUPLE 2-INPUT GATE EXPANDER	40	—	—	—	—	J
CS732	12-INPUT GATE EXPANDER	50	—	—	—	—	J

Note 1: For those items whose package type is indicated by asterisk, the NE (0°C to +70°C) series are also available in A package.

DTL

SP600 0°C to + 75°C

RECOMMENDED POWER SUPPLY 4.5 V

Introduced in late 1965, the 600 series was the first integrated circuit family to be offered in a solid, plastic, dual in-line package (DIP). It was originally available in +15°C to +55°C and 0°C to 70°C ranges. Now it is available only in a 0°C to 75°C range with improved fan-out specifications.

TYPE NUMBER	DESCRIPTION	LOGIC DIAG. REF.	FAN-OUT Function	TYPICAL CHARACTERISTICS			PACKAGE TYPE
				Tpd (ns) AND TOGGLE RATE	AVG. PWR. Function (mW) 50% Duty	DC NOISE MARGIN (V)	
SP616	DUAL 4-INPUT NAND GATE (expansion node)	10	8	30	16	1.0	A
SP620	J-K BINARY (asynchronous set and reset)	29	8	5 MHz	90	1.0	A
SP629	RS/T BINARY (asynchronous set and reset)	39	8	10 MHz	25	1.0	A
SP631	QUADRUPLE 2-INPUT GATE EXPANDER	40	—	—	—	—	A
SP659	DUAL 4-INPUT BUFFER/DRIVER (expansion node)	15	18	25	34	1.0	A
SP670	TRIPLE 3-INPUT NAND GATE	20	8	30	16	1.0	A
SP680	QUADRUPLE 2-INPUT NAND GATE	21	8	30	16	1.0	A
SP690	HEX INVERTER	87	8	30	16	1.0	A

UTILOGIC® II

SP300 0°C to +75°C
LU300 +10°C to +55°C

RECOMMENDED POWER SUPPLY
+5.0V

Utilogic II is a newly engineered version of Signetics original Utilogic family. New features include dual in-line packaging and multifunction elements, while noise margins of greater than 1-volt and high capacitive drive capability have been retained.

TYPE NUMBER	DESCRIPTION	LOGIC DIAG. REF.	FAN-OUT Function	TYPICAL CHARACTERISTICS			PACKAGE TYPE
				Tpd (ns) AND TOGGLE RATE	AVG. PWR. Function (mW) 50% Duty	DC NOISE MARGIN (mV)	
SP300 LU300	DUAL 3-INPUT EXPANDER	23	—	5	—	—	A
SP301 LU301	QUAD 2-INPUT DIODE EXPANDER	40	—	5	—	—	A
SP305 LU305	6-INPUT AND GATE	24	10	35	6.0	—	A
SP306 LU306	DUAL 3-INPUT AND GATE	25	10	35	6.0	—	A
SP314 LU314	7-INPUT NOR GATE	26	16	20	22	1200	A
SP317 LU317	DUAL 4-INPUT EXPANDABLE NOR GATE	94	16	20	22	1200	A
SP321 LU321	DUAL J-K BINARY	65	13	10 MHz	90	800	A
SP322 LU322	DUAL J-K BINARY	65	13	10 MHz	90	800	B
SP333 LU333	DUAL 3-INPUT EXPANDABLE OR GATE	95	16	35	44	1200	A
SP334 LU334	DUAL 4-INPUT EXPANDABLE OR GATE	83	16	35	22	1200	A
SP337 LU337	DUAL 4-INPUT EXPANDABLE NAND GATE	10	18	45	35	1200	A
SP356 LU356	DUAL 4-INPUT EXPANDABLE LINE DRIVER	15	28	55	37	800	A
SP362 LU362	ONE SHOT MULTIVIBRATOR	105	7	35	65	800	A
SP370 LU370	TRIPLE 3-INPUT NOR GATE	96	16	20	22	1200	A
SP374 LU374	TRIPLE 3-INPUT OR GATE	84	16	35	22	1200	A
SP375 LU375	TRIPLE 2-INPUT EXPANDABLE OR GATE	86	16	35	22	1200	A
SP377 LU377	TRIPLE 3-INPUT NAND GATE	20	18	45	35	1200	A
SP380 LU380	QUAD 2-INPUT NOR GATE	72	16	20	22	1200	A
SP384 LU384	QUAD 2-INPUT OR GATE	85	16	35	22	1200	A
SP387 LU387	QUAD 2-INPUT NAND GATE	21	18	45	35	1200	A

UTILOGIC®

SU300 −20°C to +85°C
LU300 +10°C to +55°C

RECOMMENDED POWER SUPPLY **+4.5 V**

Utilogic was introduced in 1964 as the first integrated circuit family designed specifically for industrial applications. It offers highest noise margin, high capacitive drive capability and a broad selection of logic building blocks.

TYPE NUMBER	DESCRIPTION	LOGIC DIAG. REF.	FAN-OUT Function	TYPICAL CHARACTERISTICS			PACKAGE TYPE
				Tpd (ns) AND TOGGLE RATE	AVG. PWR. Function (mW) 50% Duty	DC NOISE MARGIN (V)	
SU300 LU300	DUAL 3-INPUT GATE EXPANDER	23	—	—	—	—	G,K
SU305 LU305	6-INPUT AND GATE	24	10	25	5	—	G,K
SU306 LU306	DUAL 3-INPUT AND GATE	25	10	25	5	—	G,K
SU314 LU314	7-INPUT NOR GATE	26	17	30	18	1.2	G,K
SU315 LU315	DUAL 3-INPUT NOR GATE	27	17	30	18	1.2	G,K
SU316 LU316	DUAL 2-INPUT NOR GATE (expandable)	28	17	30	18	1.2	G,K
SU320 LU320	J-K BINARY	29	17	4 MHz	90	1.2	G,K
SU331 LU331	DUAL 2-INPUT OR GATE (expandable)	30	17	30	36	1.2	G,K
SU332 LU332	DUAL 3-INPUT OR GATE	31	17	30	36	1.2	G,K

TTL

SE400 −55°C to +125°C
NE400 0°C to + 70°C

RECOMMENDED POWER SUPPLY **+4.0 V**

This family, introduced in 1965, contains the industry's first low-power, monolithic, dual binary element, and is the first family in which TTL techniques were applied in low power circuits.

TYPE NUMBER	DESCRIPTION	LOGIC DIAG. REF.	FAN-OUT Function	TYPICAL CHARACTERISTICS			PACKAGE TYPE
				Tpd (ns) AND TOGGLE RATE	AVG. PWR. Function (mV) 50% Duty	DC NOISE MARGIN (mV)	
SE415 NE415	DUAL 5-INPUT NAND GATE (bare output collector)	32	7	32	4.5	1.0	J
SE416 NE416	DUAL 4-INPUT NAND GATE (expansion node)	15	7	30	4.5	1.0	J
SE417 NE417	DUAL 3-INPUT NAND GATE (expansion node and optional pull-up resistor)	7	7	32	4.5	1.0	J
SE424 NE424	DUAL RS/T BINARY (asynchronous reset)	33	7	9 MHz	9.0	1.0	J
SE425 NE425	DUAL RS/T BINARY (asynchronous set and reset)	59	7	9 MHz	9.0	1.0	J
SE440 NE440	DUAL AND/OR INVERT GATE	34	7	27	4.5	1.0	J
SE455 NE455	DUAL 4-INPUT BUFFER/DRIVER	14	20	30	7.0	1.0	J
SE470 NE470	TRIPLE 3-INPUT NAND GATE	35	7	27	3.5	1.0	J
SE471 NE471	TRIPLE 3-INPUT NAND GATE (bare output collector)	36	7	32	3.5	1.0	J
SE480 NE480	QUADRUPLE 2-INPUT NAND GATE	37	7	27	3.5	1.0	J
SE481 NE481	QUADRUPLE 2-INPUT NAND GATE (bare output collector)	38	7	32	3.5	1.0	J
SE490 NE490	HEX INVERTER	88	7	27	3.5	1.0	J

DCL*

S8000 −55°C to +125°C
N8000 0°C to + 75°C

RECOMMENDED POWER SUPPLY +5.0V

The concept of cross-family compatibility in integrated circuits was born in 1966 when Signetics introduced Designer's Choice Logic (DCL). This family consists of the following compatible sub-families:

8200 -- Integrated monolithic sub-systems. (MSI)

8400 -- Elements from the low-power SE400 series re-characterized for operation at 5 volts. Offers DTL logic flexibility at lower power consumption and higher fan-out than any other DTL family.

8800 -- Elements superseding the SE800 family. The classical high level TTL circuit design is utilized to provide high operating speed. This group contains six dual binaries and two single binaries.

8H00 -- A higher speed and higher power consumption version of the 8800.

8T00 -- A group of level translators to allow DCL logic elements to interface with voltage levels up to 30 volts.

TYPE NUMBER	DESCRIPTION	LOGIC DIAG. REF.	FAN-OUT Function	TYPICAL CHARACTERISTICS			PACKAGE TYPE
				Tpd (ns) AND TOGGLE RATE	AVG. PWR. Function (mW) 50% Duty	DC NOISE MARGIN (V)	
S8162 N8162	ONE-SHOT MULTIVIBRATOR (delay from 80 ns to 2 seconds)	19	12	35	65	1.0	J,A
S8230 N8230	8-INPUT DIGITAL MULTIPLEXER	100	20	20	150	1.0	R,B
S8232 N8232	8-INPUT DIGITAL MULTIPLEXER	101	20	20	160	1.0	R,B
S8241 N8241	QUAD EXCLUSIVE-OR GATE	102	20	10	50	1.0	Q,A
S8242 N8242	4 BIT COMPARATOR	103	30	10	40	1.0	Q,A
S8250 N8250	OCTAL DECODER	70	20	20	85	1.0	J,A
S8251 N8251	DECIMAL DECODER	70	20	20	95	1.0	B
S8260 N8260	ARITHMETIC LOGIC ELEMENT	92	12	12	90/bit	1.0	P
S8261 N8261	FAST CARRY EXTENDER	93	12	5	90	1.0	Q,A
S8266 N8266	4 BIT— 2-INPUT DIGITAL MULTIPLEXER	104	20	10	45	1.0	R,B
S8267 N8267	4 BIT— 2-INPUT DIGITAL MULTIPLEXER (bare collector output)	104	20	10	45	1.0	R,B
S8270 N8270	4-BIT SHIFT REGISTER (parallel entry)	71	14	20	165	1.0	Q,A
S8271 N8271	4-BIT SHIFT REGISTER (parallel entry)	71	14	20	165	1.0	B
S8280 N8280	DECADE COUNTER/STORAGE REGISTER	60	8	35 MHz	25/bit	1.0	J,A
S8281 N8281	BINARY COUNTER/STORAGE REGISTER	61	8	35 MHz	25/bit	1.0	J,A
S8284 N8284	SYNCHRONOUS BINARY UP/DOWN COUNTER	98	12	30 MHz	60/bit	1.0	Q,A
S8285 N8285	SYNCHRONOUS DECADE UP/DOWN COUNTER	99	12	30 MHz	60/bit	1.0	Q,A
S8415 N8415	DUAL 5-INPUT NAND GATE (bare collector output)	32	9	30	10.0	1.0	J,A
S8416 N8416	DUAL 4-INPUT NAND GATE (input expansion node)	15	9	25	10.0	1.0	J,A
S8417 N8417	DUAL 3-INPUT NAND GATE (expansion node and optional output resistor)	7	9	30	9.5	1.0	J,A
S8424 N8424	DUAL, LOW POWER, RS/T BINARY (trailing edge triggered)	33	9	11 MHz	15.5	1.0	J,A
S8425 N8425	DUAL LOW POWER RS/T BINARY (trailing edge triggered)	59	9	11 MHz	15.5	1.0	J,A
S8440 N8440	DUAL AND-OR-INVERT GATE (2 AND gates wide)	34	9	25	12.0	1.0	J,A
S8455 N8455	DUAL 4-INPUT NAND GATE/DRIVER	14	25	28	11.0	1.0	J,A
S8470 N8470	TRIPLE 3-INPUT NAND GATE	35	9	25	7.0	1.0	J,A
S8471 N8471	TRIPLE 3-INPUT NAND GATE (bare collector output)	36	9	30	7.0	1.0	J,A

*Signetics Trademark

TYPE NUMBER	DESCRIPTION	LOGIC DIAG. REF.	FAN-OUT Function	TYPICAL CHARACTERISTICS			PACKAGE TYPE
				Tpd (ns) AND TOGGLE RATE	AVG. PWR. Function (mW) 50% Duty	DC NOISE MARGIN (V)	
S8480 N8480	QUADRUPLE 2-INPUT NAND GATE	37	9	25	7.0	1.0	J,A
S8481 N8481	QUADRUPLE 2-INPUT NAND GATE (bare collector output)	38	9	30	7.0	1.0	J,A
S8490 N8490	HEX INVERTER	88	9	25	7.0	1.0	J,A
S8706 N8706	DUAL 5-INPUT DIODE EXPANDER	41	—	—	—	—	J,A
S8731 N8731	QUADRUPLE 2-INPUT DIODE EXPANDER	40	—	—	—	—	J,A
S8806 N8806	DUAL 4-INPUT EXPANDER	51	—	—	—	—	J,A
S8808 N8808	8-INPUT NAND GATE	52	20	8	13	1.0	J,A
S8815 N8815	DUAL 4-INPUT NOR GATE	89	20	8	30	1.0	J,A
S8816 N8816	DUAL 4-INPUT NAND GATE	14	20	8	13	1.0	J,A
S8821 N8821	DUAL HIGH SPEED J-K BINARY (trailing edge triggered)	65	20	25 MHz	56	1.0	J
S8822 N8822	DUAL HIGH SPEED J-K BINARY (trailing edge triggered)	65	20	25 MHz	56	1.0	J,A
S8824 N8824	DUAL HIGH SPEED J-K BINARY (trailing edge triggered)	65	20	25 MHz	56	1.0	B
S8825 N8825	SINGLE PHASE, AND INPUT J-K BINARY (leading edge triggered)	62	20	25 MHz	70	1.0	J,A
S8826 N8826	DUAL HIGH SPEED J-K BINARY (trailing edge triggered)	53	10	30 MHz	40	1.0	J,A
S8827 N8827	DUAL HIGH-SPEED J-K BINARY (full asynchronous entry, trailing edge triggered)	54	10	30 MHz	40	1.0	J,A
S8828 N8828	DUAL HIGH SPEED "D" TYPE BINARY (leading edge triggered)	63	20	25 MHz	55	1.0	J,A
S8829 N8829	SINGLE PHASE AND INPUT J-K BINARY (trailing edge triggered)	64	20	20 MHz	75	1.0	J,A
S8840 N8840	DUAL AND-OR-INVERT GATE (2 AND gates wide)	55	20	8	15	1.0	J,A
S8848 N8848	AND-OR-INVERT GATE (4 AND gates wide)	56	20	8	30	1.0	J,A
S8855 N8855	DUAL 4-INPUT POWER GATE	14	60	8	24	1.0	J,A
S8870 N8870	TRIPLE 3-INPUT NAND GATE	35	20	8	13	1.0	J,A
S8875 N8875	TRIPLE 3-INPUT NOR GATE	90	20	8	30	1.0	J,A
S8880 N8880	QUADRUPLE 2-INPUT NAND GATE	37	20	8	13	1.0	J,A
S8881 N8881	QUADRUPLE 2-INPUT NAND GATE (bare output collector)	38	20	18	13	1.0	J,A
S8885 N8885	QUADRUPLE 2-INPUT NOR GATE	91	20	8	30	1.0	J,A
S8H16 N8H16	DUAL 4-INPUT NAND GATE (high-speed)	14	30	5	20	1.0	J,A
S8H20 N8H20	DUAL J-K BINARY	66	30	80	60	1.0	Q
S8H21 N8H21	DUAL J-K BINARY	68	30	80	60	1.0	Q,A
S8H22 N8H22	DUAL J-K BINARY	67	30	80	60	1.0	B
S8H70 N8H70	TRIPLE 3-INPUT NAND GATE (high-speed)	35	30	5	20	1.0	J,A
S8H80 N8H80	QUADRUPLE 2-INPUT NAND GATE (high-speed)	37	30	5	20	1.0	J,A
S8H90 N8H90	HEX INVERTER (high-speed)	88	30	5	20	1.0	Q,A
S8T01 N8T01	DECODER-NIXIE* DRIVER	69	Output Rating: 68 V		60	—	B
S8T18 N8T18	DUAL 2-INPUT NAND INTERFACE GATE (high voltage to low voltage)	57	9	15	45	7.0	J,A
S8T80 N8T80	QUADRUPLE 2-INPUT NAND INTERFACE GATE (low voltage to high voltage)	38	9	25	10.0	1.0	J,A
S8T90 N8T90	HEX INVERTER INTERFACE ELEMENT (low voltage to high voltage)	58	9	25	10.0	1.0	J,A

*Burroughs Corp. Trademark

TTL

S5400 −55°C to +125°C
N7400 0°C to + 70°C

RECOMMENDED POWER SUPPLY **+5.0 V**

Signetics 5400/7400 TTL provide superior performance in existing system designs requiring the logic configuration and pin connections presented by this logic family. For new system designs, the system designer is referred to Signetics DCL product family.

TYPE NUMBER	DESCRIPTION	LOGIC DIAGRAM	FAN-OUT	TYPICAL CHARACTERISTICS			PACKAGE TYPE
				T_{pd} (ns) TOGGLE RATE	AVG. POWER Per Function (mW) 50% Duty	DC NOISE MARGIN (V)	
S5400 N7400	QUADRUPLE 2-INPUT NAND	37	10	8	13	1.0	J/A
S5401 N7401	QUADRUPLE 2-INPUT NAND (Open Collector Output)	72	10	18	13	1.0	J/A
S5402 N7402	QUADRUPLE 2-INPUT NOR	72	10	8	20	1.0	J/A
S5410 N7410	TRIPLE 3-INPUT NAND	35	10	8	13	1.0	J/A
S5420 N7420	DUAL 4-INPUT NAND	14	10	8	13	1.0	J/A
S5430 N7430	SINGLE 8-INPUT NAND	52	10	8	13	1.0	J/A
S5440 N7440	DUAL 4-INPUT NAND BUFFER	14	30	8	24	1.0	J/A
N7441	BCD-TO-DECIMAL DECODER DRIVER	73	OUTPUT RATING = 55 V		75	—	B
S5450 N7450	DUAL 2-WIDE 2-INPUT AND OR-INVERT, EXPANDABLE	55	10	8	15	1.0	J/A
S5451 N7451	DUAL 2-WIDE 2-INPUT AND-OR-INVERT	34	10	8	15	1.0	J/A
S5453 N7453	4-WIDE 2-INPUT AND-OR-INVERT, EXPANDABLE	74	10	8	30	1.0	J/A
S5454 N5454	4-WIDE 2-INPUT AND-OR-INVERT	75	10	8	30	1.0	J/A
S5460 S7460	DUAL 4-INPUT EXPANDER	51	—	—	—	—	J/A
S5470 N7470	J-K FLIP-FLOP	76	10	25 MHz	85	1.0	J/A
S5472 N7472	J-K MASTER-SLAVE FLIP-FLOP	77	10	15 MHz	85	1.0	J/A
S5473 N7473	DUAL J-K MASTER-SLAVE FLIP-FLOP	78	10	15 MHz	50	1.0	J/A
S5474 N7474	DUAL D-TYPE, EDGE-TRIGGERED, FLIP-FLOP	79	10	25 MHz	70	1.0	J/A
S5475 N7475	QUADRUPLE BISTABLE LATCH	80	10	—	175	1.0	B
S5476 N7476	DUAL J-K MASTER-SLAVE FLIP-FLOP W/PRESET & CLEAR	81	10	15 MHz	40	1.0	B
S5480 N7480	GATED FULL ADDER	97	10	62	110	1.0	Q/A
S5491 N7491	8-BIT SHIFT REGISTER	82	10	18 MHz	175	1.0	Q/A

LINEAR

S5700, SE500 −55°C to +125°C
N5700, NE500 0°C to + 70°C

Signetics linear products provide all of the most frequently required circuit functions over a broad spectrum of gain and bandwidth combinations.

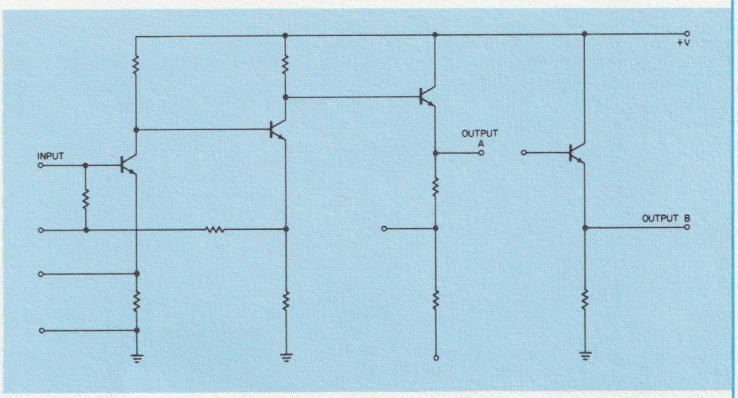
AMPLIFIERS: VIDEO, IF/RF

SE501, NE501 Video Amplifier

The 501 is a wide-band video amplifier featuring low voltage operation (+6V) and is useful to 150 MHz. Internal feedback resistors are available for gain-bandwidth adjustment. Typical applications include tuned circuit amplifiers, pulse amplifiers, and local oscillators.

Features:

• Low Voltage Operation	+6 V
• Unity Gain Frequency	150 MHz
• Noise Figure	5 dB
• Low Output Impedance	18 Ω
• Power Dissipation	20 mW
• Voltage Gain Stability	±0.5 dB
• Package	A, G, K



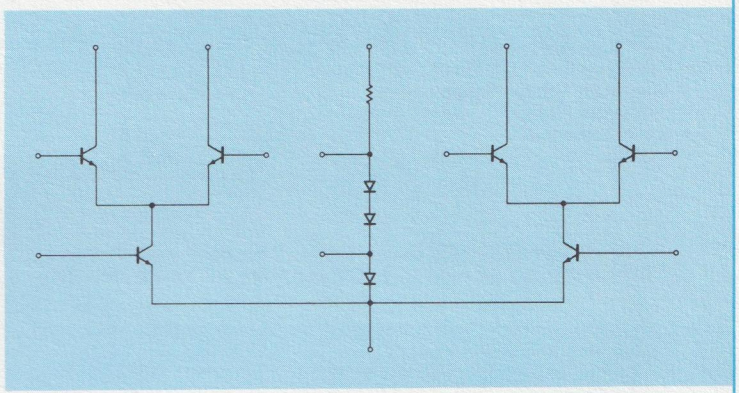
SE510, NE510 Dual RF/IF Amplifier

The 510 is a dual high frequency amplifier intended for use from DC to beyond 100 MHz. The differential amplifiers with internal constant current sources and biasing elements provide extreme flexibility. Circuit layout provides for connection as either CE-CB, CC-CB, or high gain differential amplifier. Typical applications include tuned circuits, modulators, oscillators, AGC amplifiers, and comparators.

Features:

• Low Offset Voltage	±2 mV
• Low Offset Current	±3 μA
• Single Power Supply	
• AGC Capability	
• Internal Biasing	

Dynamic Characteristics:	**CC-CB** Common-Collector, Common-Base Connection	**CE-CB** Common-Emitter, Common-Base Connection
Forward Transconductance (G_{21})	25 mmho	75 mmho
Input Conductance (G_{11})	0.7 mmho	2.0 mmho
Input Capacitance	4.5 pF	10 pF
Output Conductance (G_{22})	0.01 mmho	0.01 mmho
Output Capacitance	2.5 pF	2.5 pF
Reverse Transfer Capacitance	0.05 pF	0.05 pF
Package		A, J



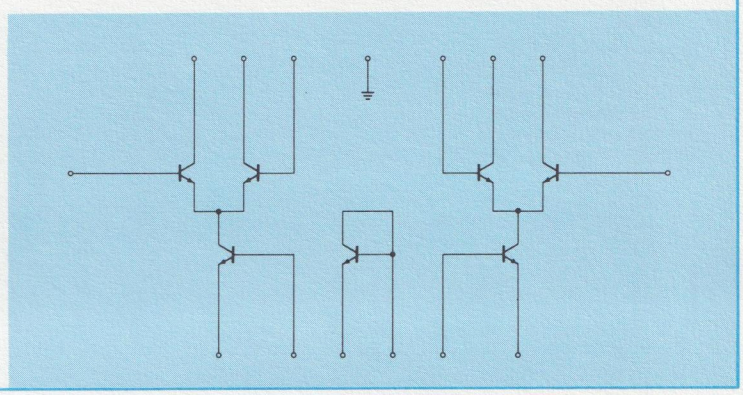
SE511, NE511 Dual RF/IF Amplifier

The 511 is a dual high-frequency amplifier intended to complement the 510. Additional internal points are brought out to allow independent emitter degeneration to increase linearity and minimize distortion. Applications include tuned circuits, modulators, limiters, and high-speed comparators.

Features:

• Low Offset Voltage	±2 mV
• Low Offset Current	±3 μA
• Single Power Supply	
• AGC Capability	

Dynamic Characteristics:	**CC-CB** Common-Collector, Common-Base Connection	**CE-CB** Common-Emitter, Common-Base Connection
Forward Transconductance (G_{21})	25 mmho	75 mmho
Input Conductance (G_{11})	0.7 mmho	2.0 mmho
Input Capacitance	4.5 pF	10 pF
Output Conductance (G_{22})	0.01 mmho	0.01 mmho
Output Capacitance	2.5 pF	2.5 pF
Reverse Transfer Capacitance	0.05 pF	0.05 pF
Package		B



LINEAR

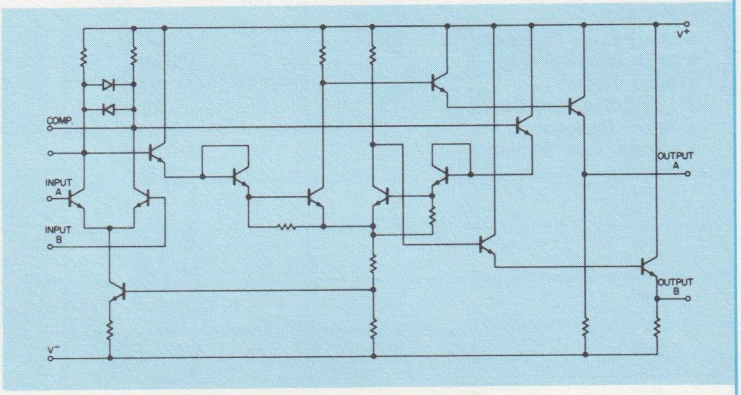
AMPLIFIERS: OPERATIONAL

SE515, NE515 Differential Amplifier

The 515 is a high gain wideband amplifier with a differential input and differential output. The dual output allows easy use of feedback circuitry. Its high common mode range at low operating voltages makes the 515 superior for low power, low voltage applications. Typical applications include summing amplifiers, integrators, DC amplifiers, and logarithmic amplifiers.

Features:

• High Common Mode Range	
• Low Voltage Operation	+6 V, −3 V or +4 V, −2 V
• Low Input Offset Voltage	0.5 mV
• Bandwidth	1 MHz
• Differential Output	
• Offset Voltage Stability	5 μV/°C
• Voltage Gain	4500
• Package	A, G, K

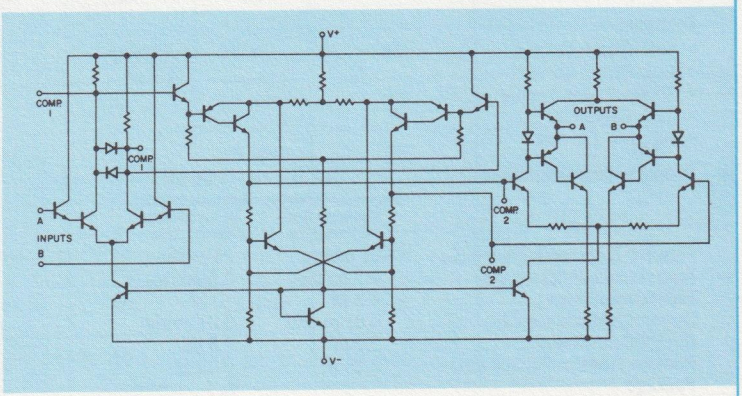


SE516, NE516 Operational Amplifier

The 516 is a high-gain operational amplifier with differential input and differential output. It requires only a single capacitor and resistor for frequency compensation, and its dual output provides excellent design versatilities. The 516 will meet general op-amp requirements for use in DC servos, summing amplifiers, and integrators.

Features:

• High Open Loop Gain	18,000
• High Output Voltage Swing	±11 V
• High Input Voltage Range	+10, −13 V
• Differential Output	
• Input Impedance	400 K
• Package	A, G, K

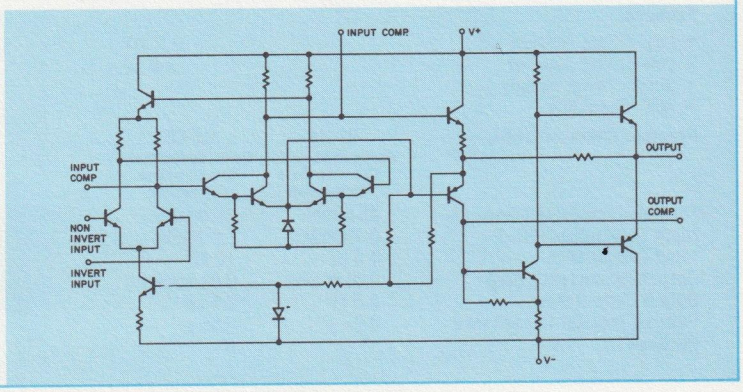


S5709, N5709 Operational Amplifier

The 5709 is a high performance operational amplifier and is a pin-for-pin replacement for the μA709 operational amplifier. Its low temperature drift characteristics and high input and output voltage ranges make it extremely versatile. Typical applications include DC amplifiers, voltage regulators, integrators, differentiators, and oscillators.

Features:

• Input Offset Voltage	1.0 mV
• Open Loop Voltage Gain	45,000
• Output Voltage Swing	±14 V
• Input Voltage Swing	±10 V
• Input Offset Current	50 nA
• Input Impedance	400 K
• Package	A, G, T



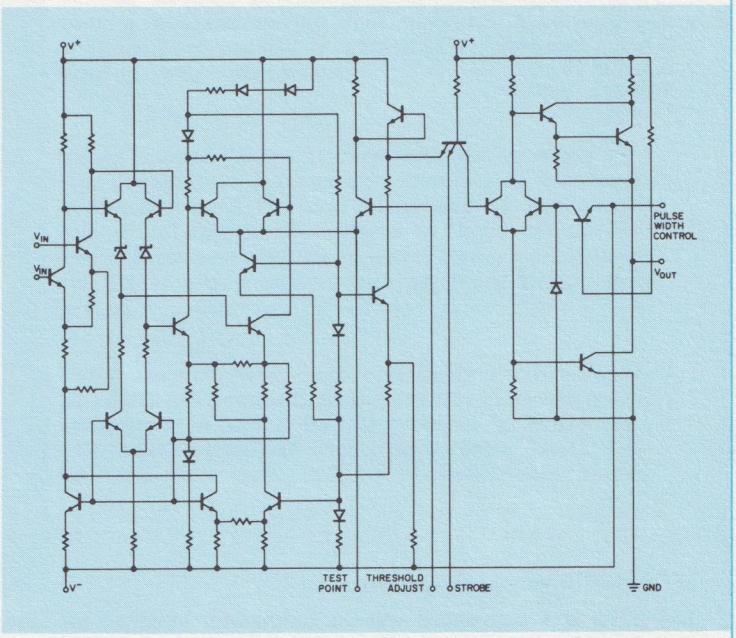
CORE MEMORY SENSE AMPLIFIER

NE525 Core Memory Sense Amplifier

The 525 is a high speed core memory sense amplifier specifically designed for memories operating down to 400 ns. The ±2 mV uncertainty range is unique and available only in the 525. The circuit operates off ± 5V power supplies and features a TTL gate output which is compatible with DCL, DTL, and TTL current and voltage requirements.

Features:

• Uncertainty Range	±2 mV
• Propagation Delay	30 ns
• Low Power Consumption	110 mW
• High Common Mode Range	+4.5 V, −3.5 V
• Power Supply	±5 V
• Package	A, J



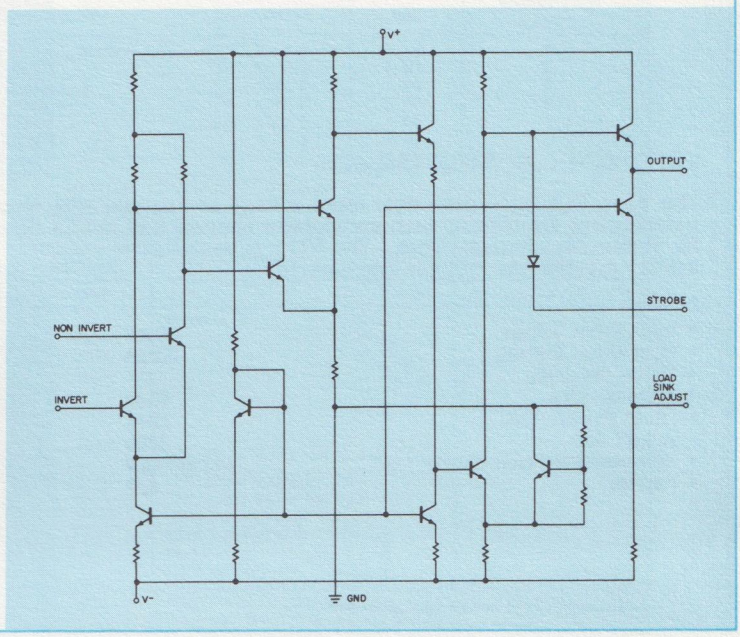
VOLTAGE COMPARATORS

SE518, NE518 Voltage Comparator

The 518 is a high speed voltage comparator. Its unique strobe control, and load sink adjust, make the 518 useful not only as a comparator but also as a sense amplifier, Schmitt trigger and line driver. In addition, the 518 can be operated with low voltage power supplies +4V, −2V.

Features:

• Strobe Capability	
• Input Offset Voltage	1.0 mV
• Bandwidth	5.0 MHz
• Response Time	40 ns
• Low Voltage Operation	+6 V, −3 V or +4 V, −2 V
• Voltage Gain	2100
• Package	A, G, K



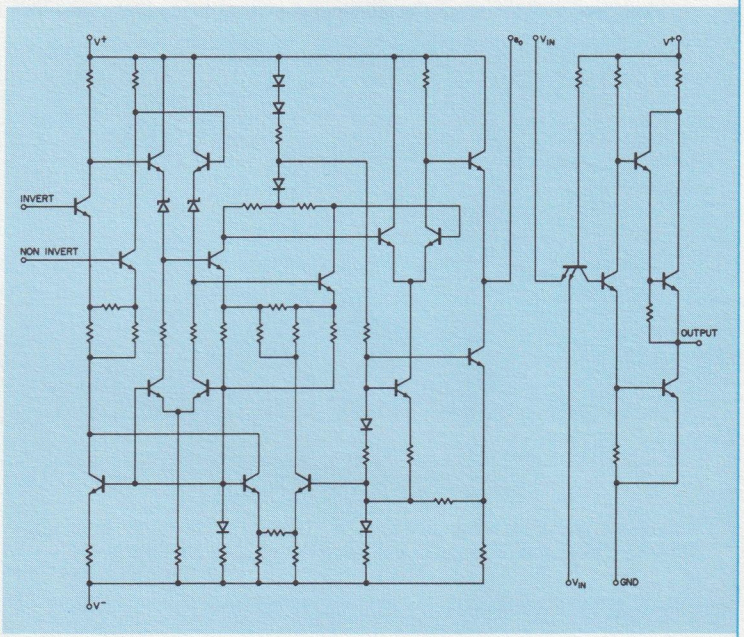
LINEAR

SE526, NE526 High Speed Comparator/Sense Amplifier

The 526 analog comparator is intended for use in systems where speed, wide common mode range, and low power consumption are required. Its output is compatible with DCL, DTL and TTL and features a fanout of 10. The 526 reduces can count and eliminates power supplies. Typical applications include Schmitt Triggers, analog comparators and clock generators.

Features:

- Operates from Standard ±5 V Supplies
- Propagation Delay — 30 ns
- Overdrive Recovery — 20 ns
- Fanout of 10
- High Gain Operation
- Package — A, G, K

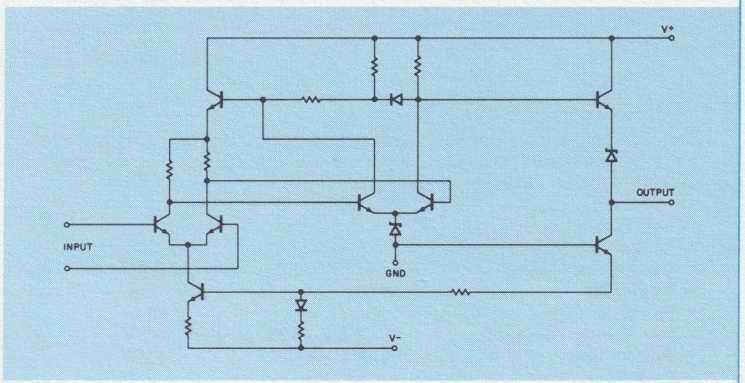


S5710, N5710 Voltage Comparator

The 5710 is a high-speed voltage comparator intended for systems requiring low offset voltage and wide input voltage range. It is a pin-for-pin replacement for the μA710 and is available at extremely low cost. Typical applications include line receivers, Schmitt triggers, and threshold detectors.

Features:

- Low Input Offset Voltage — 0.6 mV
- Low Input Offset Current — 0.75 μA
- Response Time — 40 ns
- Offset Voltage Stability — 3.5 μV/°C
- Input Common Mode Range — ±5 V
- Package — A, G, T

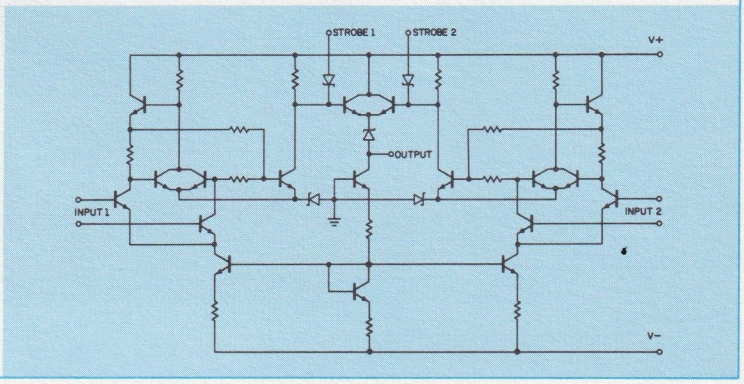


S5711, N5711 Dual Voltage Comparator

The 5711 is a high-speed dual input voltage comparator with strobe capability. It is a pin-for-pin replacement for the μA711. Independent strobing of each comparator channel and output compatibility with all forms of integrated logic forms complement its stable DC characteristics. The 5711 is useful as a sense amplifier and multiple line detector.

Features:

- Input Offset Voltage — 1.0 mV
- Input Offset Current — 0.5 μA
- Strobe Capability
- Response Time — 40 ns
- Strobe Release Time — 12 ns
- Voltage Gain — 1500
- Recommended Power Supply — +12 V, −6 V
- Package — A, K



SIGNETICS SURE* PROGRAM

The Signetics SURE* Program consists of a combination of 100 percent and statistical sample tests designed to assure specified performance, continuing uniformity, and long term reliability in Signetics products. These tests are made regularly at no extra cost to the user and are performed in addition to the 17 quality assurance inspections and tests to which every circuit is subjected before final seal. The tests, tabulated below for the specifier's convenience, are performed in accordance with the following conditions, sequence, and schedules on equipment calibrated to meet all requirements of MIL-Q-9858A and MIL-C-45662A.

Every circuit of every lot is processed to the environmental screens shown in Table I. These screens are performed in production, subsequent to assembly and just prior to 100 percent final production electrical tests. Any unit failing either the environmental screens or the final production electrical tests is rejected and removed from the lot.

After completion of Table I tests, each manufacturing lot is sampled and tested by Quality Assurance for conformance to the requirements of Table II. The unsampled portion of the lot is held pending acceptance of the lot sample. Detailed electrical test limits and conditions applicable to each subgroup are shown in the Electrical Characteristics table of the individual part type data sheets.

Group B Inspection shown in Table III is a complete environmental series in accordance with MIL-S-19500 and MIL-STD-750. These tests are performed once in every 28-day manufacturing period on a production lot of a representative circuit type. The circuit type selected each period is changed routinely and is representative of all structurally similar devices produced on the same line by the same processes during that period. A summary of these test results is available on request at the time of order placement.

Group C tests (Table IV) are intended to verify design parameters that are not specifically measured in Group A or B but are guaranteed by consideration of related measurements in those two series. These tests are performed every 90 days on at least one lot of every circuit type produced during that period.

For those with ultra-high reliability requirements, an additional preconditioning series, including operating burn-in and X-Ray, applicable to every circuit to be shipped, is available at extra cost. Details are given under Optional Preconditioning Series (Table V).

TABLE I — 100% PRODUCTION SCREEN TESTS

Thermal Shock:	5 cycles; 60 seconds at 0°C, 60 seconds at 100°C, transfer time 5 seconds (G, J, P, Q, R packages only)
Centrifuge:	y_1 axis; 30,000 g minimum (G, J, K, P, Q, R packages only)
Hermeticity:	Gross leak test (G, J, P, Q, R packages only)

Above series performed prior to FINAL ELECTRICAL TESTS

TABLE II — GROUP A, PRODUCT ACCEPTANCE TESTS

SUB-GROUP	TEST	CONDITIONS	LIMITS	AQL	INSPECTION LEVEL
A-1	Visual and Mechanical Inspection	Per MIL-STD-750, Method 2071	Note 2	1.0%	II
A-2	DC Parameters	T = +25°C; Note 1	Note 2	1.0%	II
A-3	DC Parameters	T = +25°C; Notes 1, 3	Note 2	1.0%	II
A-4	DC Parameters	T = +125°C; Note 1	Note 2	1.0%	II
A-5	DC Parameters	T = -55°C; Note 1	Note 2	1.0%	II
A-6	AC Parameters	T = +25°C; Note 1	Note 2	1.0%	II

TABLE III — GROUP B, ENVIRONMENTAL QUALIFICATION TESTS PER MIL-S-19500D

SUB-GROUP	TEST	CONDITIONS	MIL-STD-750 METHOD	LIMITS	LTPD	MAX. ACCEPTANCE NUMBER
B-1	Physical Dimensions		2066		15	1
B-2	DC Parameters	Per GROUP A, SUB-GROUP 3		Notes 2, 3		
	Solderability	All terminals	2026			
	Temperature Cycling	10 cycles, T_{max}=+175°C	1051			
	Thermal Shock	T_{min}=-70°C T_{max}=+100°C 5 cycles, 1 minute at each extreme Transfer time = 5 sec. max.	1056			
	Moisture Resistance	Omit initial conditioning	1021		15	1
	Electrical End Points	Per GROUP A, SUB-GROUP 3		Notes 2, 3		
	FAILURE CRITERIA	"1" Input Current		10X Initial Value for DTL 5X Initial Value for TTL		
		"1" Output Voltage		±20% Initial Value		
		"0" Input Current		±20% Initial Value		
		"0" Output Voltage		±0.1V		
		Expansion Node Current (as applicable)		±20% Initial Value		

*Systematic Uniformity and Reliability Evaluation

SUB-GROUP	TEST	CONDITIONS	MIL-STD-750 METHOD	LIMITS	LTPD	MAX. ACCEPTANCE NUMBER
B-3	DC Parameters	Per GROUP A, SUB-GROUP 3		Notes 2, 3		
	Shock	1500g; 5 blows ea. x_1, y_1, z_1; 0.5ms	2016			
	Vibration Fatigue	30 g; non-operating	2046			
	Vibration, Var. Freq.	30 g;	2056		15	1
	Acceleration	30,000 g; 1 min. ea. x_1, y_1, z_1	2006			
	Electrical End Points	Per GROUP A, SUB-GROUP 3		Notes 2, 3		
	FAILURE CRITERIA	Same as B-2				
B-4	Terminal Strength	Test Condition E; weight = 4 oz.	2036			
	Hermeticity *	Per MIL-STD-202, Method 112C				
	Small Leak	Condition C; Procedure 111A		5×10^{-8} cc/sec. max.	15	1
	Large Leak	Condition A; Ethylene Glycol				
B-5	Salt Atmosphere		1041		15	1
B-6	DC Parameters	Per GROUP A, SUB-GROUP 3		Notes 2, 3		
	Storage Life	1000 hours at T_{min}=+150°C	1031		λ=15	
	Electrical End Points	Per GROUP A, SUB-GROUP 3		Notes 2, 3		
	FAILURE CRITERIA	Same as B-2				
B-7	DC Parameters	Per GROUP A, SUB-GROUP 3		Notes 2, 3		
	Operating Life	1000 hours at T_{min}=+125°C;	1026			
		Dynamic operating at 100 KHz			λ=10	
	Electrical End Points	Per GROUP A, SUB-GROUP 3		Notes 2, 3		
	FAILURE CRITERIA	Same as B-2				

TABLE IV — GROUP C, DESIGN TESTS

SUB-GROUP	TEST	CONDITIONS	LIMITS	AQL	INSPECTION LEVEL
C-1	DC Parameters	Note 1	Note 2	1.0%	II
C-2	AC Parameters	Note 1	Note 2	1.0%	II

OPTIONAL HIGH RELIABILITY SCREENING

To maximize reliability in critical applications the Optional High Reliability Screening Series of Table V provides for 100 percent screening at extra cost. This series eliminates the necessity for special specifications, minimizes cost and provides the shortest possible delivery time. This series is applied after the normal GROUP A acceptance tests. Circuits subjected to this PRECONDITIONING SERIES are clearly distinguishable from standard products in the following ways:

1. Individual serial number on each circuit.
2. First letter of part number is R, i.e., RE180J.
3. Individual device variable parameter test data supplied with each shipment.

Consult your local representative for price information. Device types should be specified with R prefixes when ordering.

TABLE V — OPTIONAL HIGH RELIABILITY SCREENING

TEST	CONDITIONS	MIL-STD-750 METHOD	LIMITS	LEVEL
Thermal Shock	T_{min} = -70°C T_{max} = +100°C 5 cycles; 1 minute at each extreme Transfer Time = 5 sec. max.	1056		100%
Mechanical Shock	1500 g; 5 blows y_1; 0.5ms (G, J, K, P, Q, R packages only)	2016		100%
Centrifuge	30,000 g, y_1 (G, J, K, P, Q, R packages only)	2006		100%
Hermeticity *	Per MIL-STD-202, Method 112C			100%
Small Leak	Condition C, Procedure III a		5×10^{-8} cc/sec.	
Large Leak	Condition A, Ethylene Glycol			
Visual Inspection		2071		100%
DC Parameters	Per GROUP A, SUB-GROUP 3; Record Data		Notes 2, 3	100%
Capacitor Stress	24 hours; T_{min} = +125°C; DC Condition		Note 4	100%
Operating Burn-In	168 hours, +12 hrs. - 0 hr.; T_{min} = +125°C Dynamic operation at 100KHz	1026		100%
DC Parameters	Per GROUP A, SUB-GROUP 3; Record Data Apply failure criteria		Notes 2, 3	100%
GROUP A	Sample lot per Table II and perform A-2, A-4, A-5 and A-6 tests.		Note 2	A.Q.L. = 1.0% Level II
X-Ray	Per Signetics Specification 871004			100%
Visual Inspection		2071		100%

Notes:

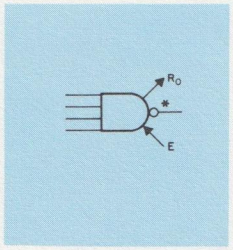
1. All test equipment calibrated to meet requirements of MIL-Q-9858A and MIL-C-45662A.
2. Detailed tests, conditions, and limits applicable to each sub-group are given in data sheet ELECTRICAL CHARACTERISTICS table.
3. These specific tests are used to determine Electrical End Points as required in GROUP B and OPTIONAL PRECONDITIONING SERIES.
4. Applicable only to device types incorporating MOS capacitors.

* For silicone molded package integrated circuits, the MIL-STD-202, Method 112 hermeticity tests are not employed due to the product's solid package construction. For subgroup B4, a 1-hour, 50 psi detergent bomb test has been incorporated into the SURE Program for this product. Test methods are being evaluated in order to determine a suitable nondestructive seal integrity test for inclusion into the Table V 100% screening series.

LOGIC DIAGRAMS

DEFINITIONS

A = Active pull-up. Do not use collector logic.
R_O = Pull-up resistor brought out for optional use. For collector logic, at least one resistor per array must be used.
E = Expansion node.
R = Internally connected pull-up resistor. Collector logic permissible.
* = Bare output collector.



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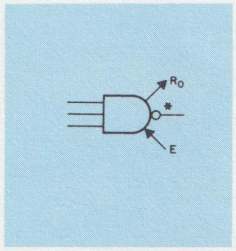

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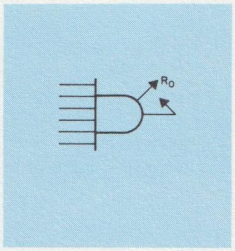

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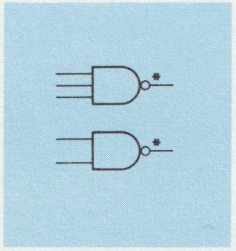

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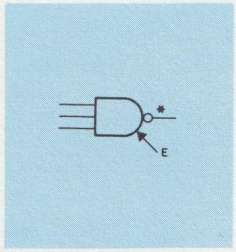

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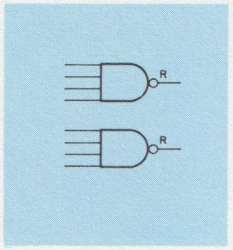

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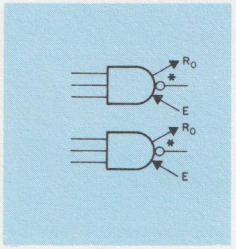

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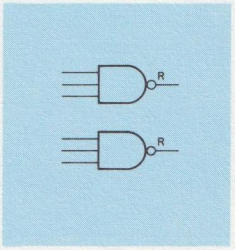

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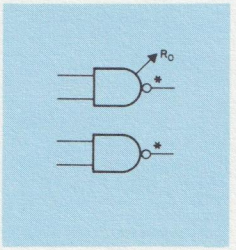

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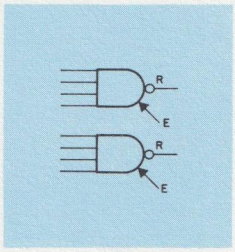

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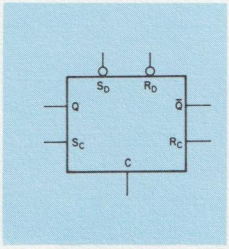

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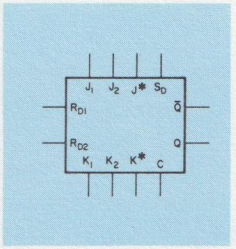

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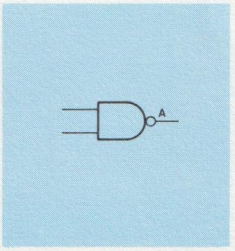

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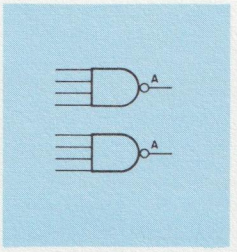

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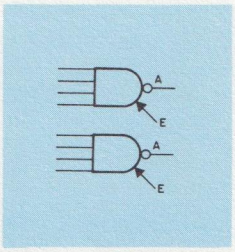

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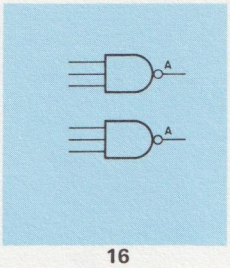

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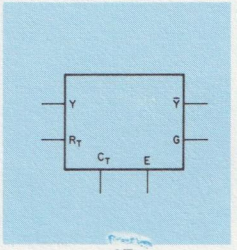

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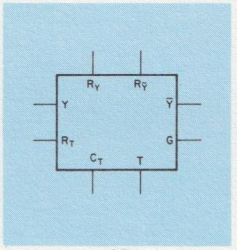

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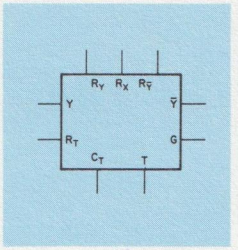

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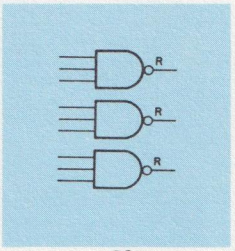

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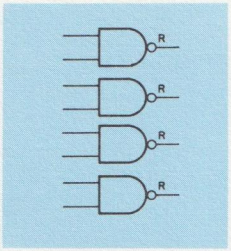

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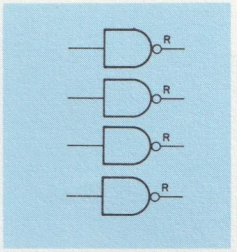

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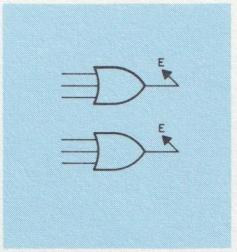

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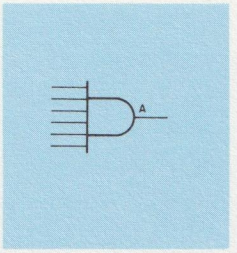

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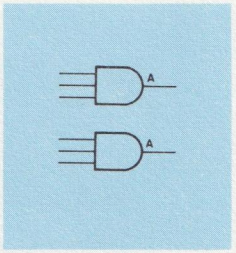

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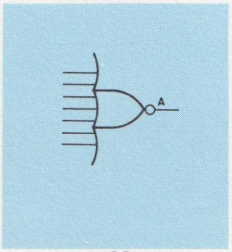

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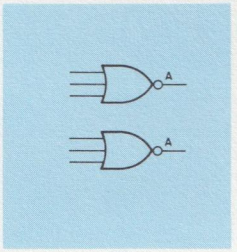

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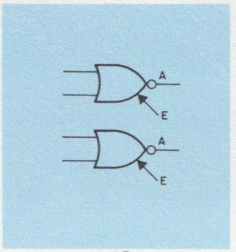

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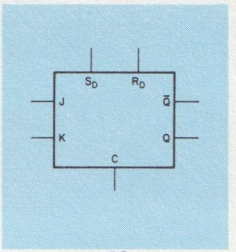

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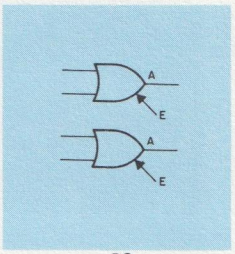

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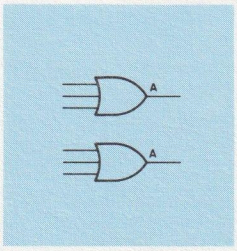

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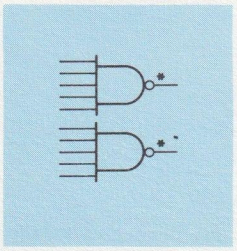

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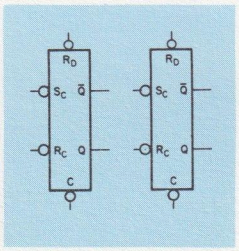

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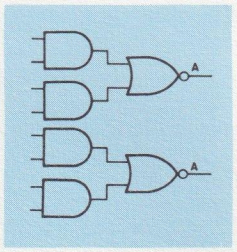

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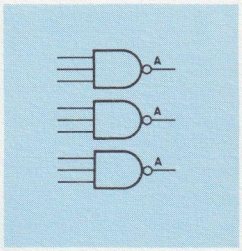

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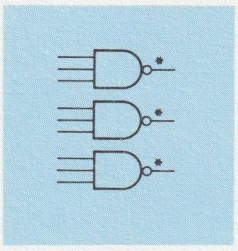

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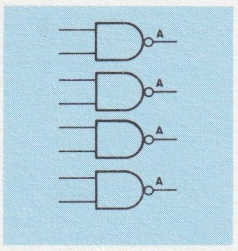

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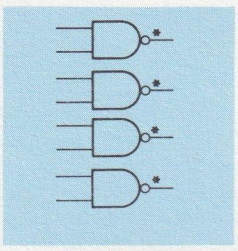

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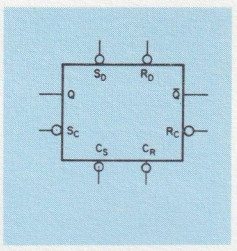

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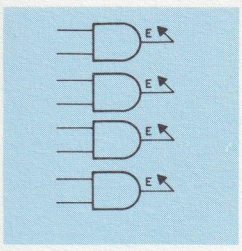

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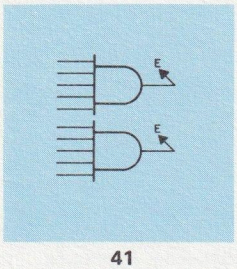

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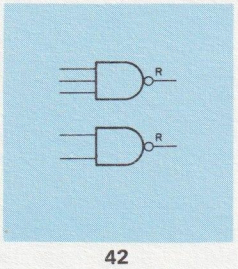

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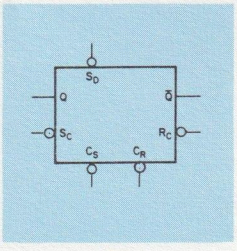

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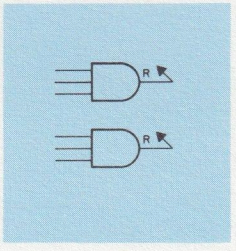

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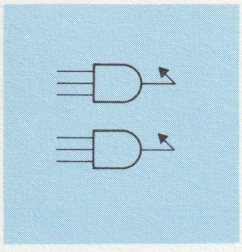
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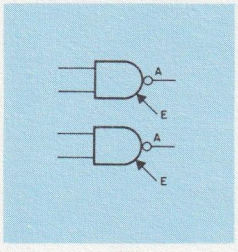

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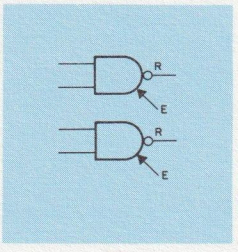

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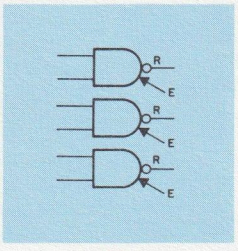

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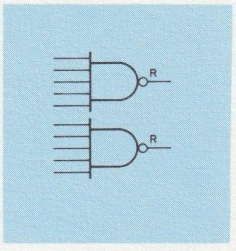

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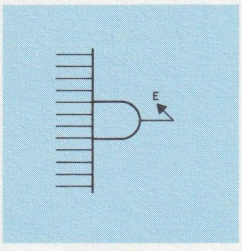

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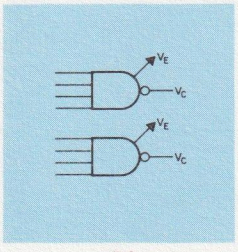

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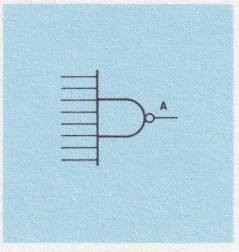

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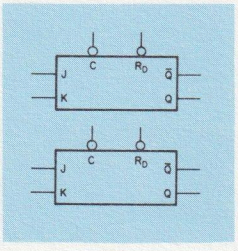

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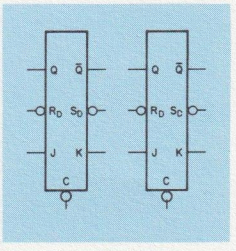

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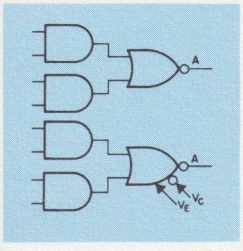

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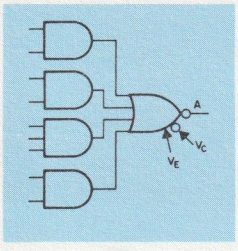

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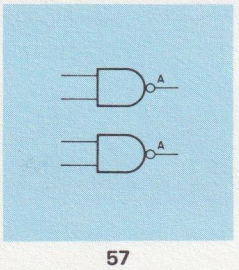

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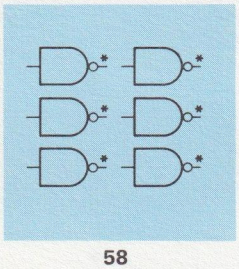

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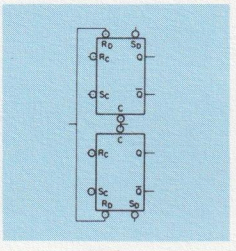

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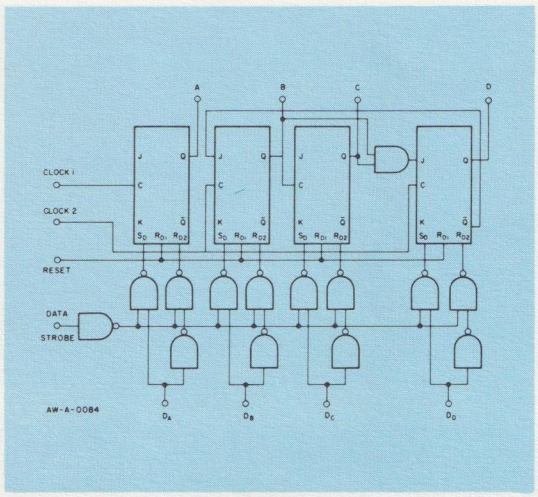

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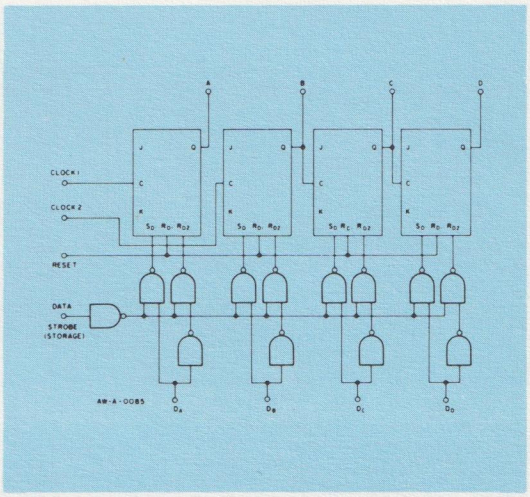

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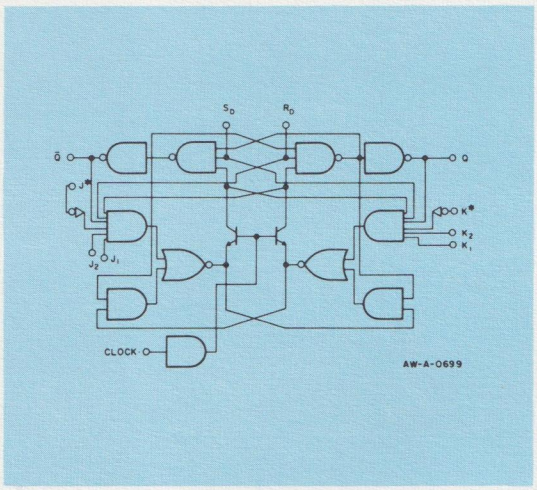

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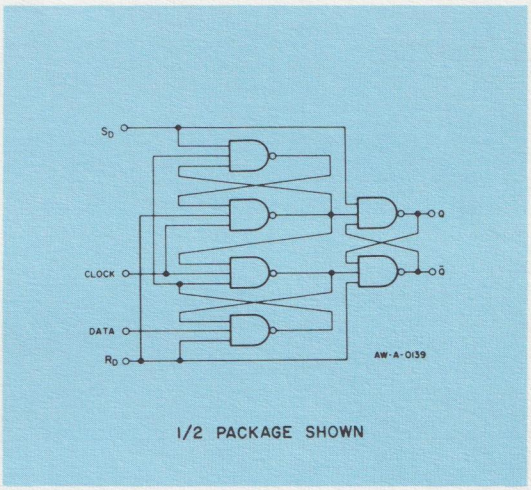

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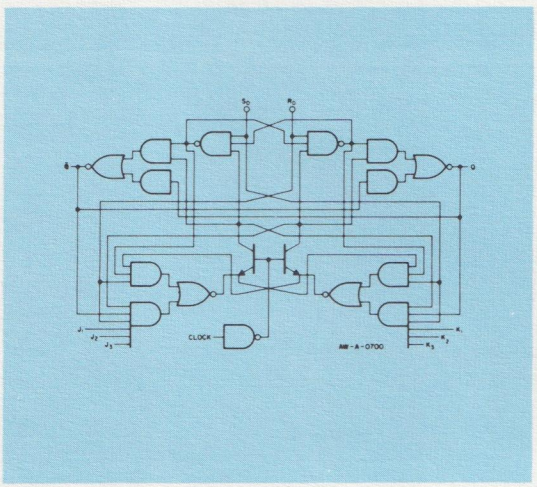

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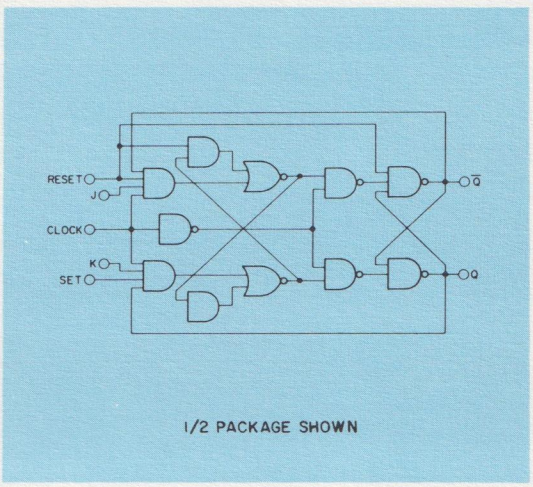

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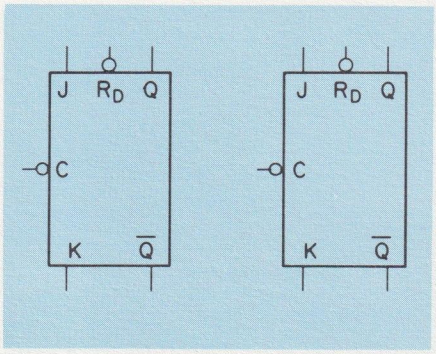

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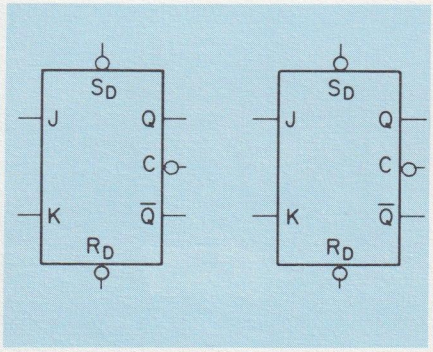

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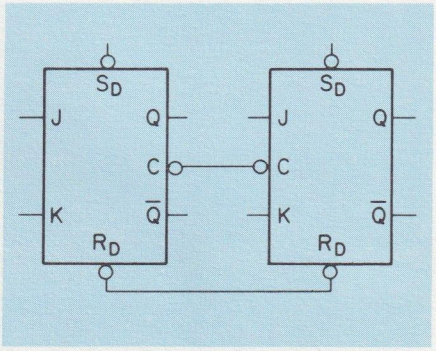

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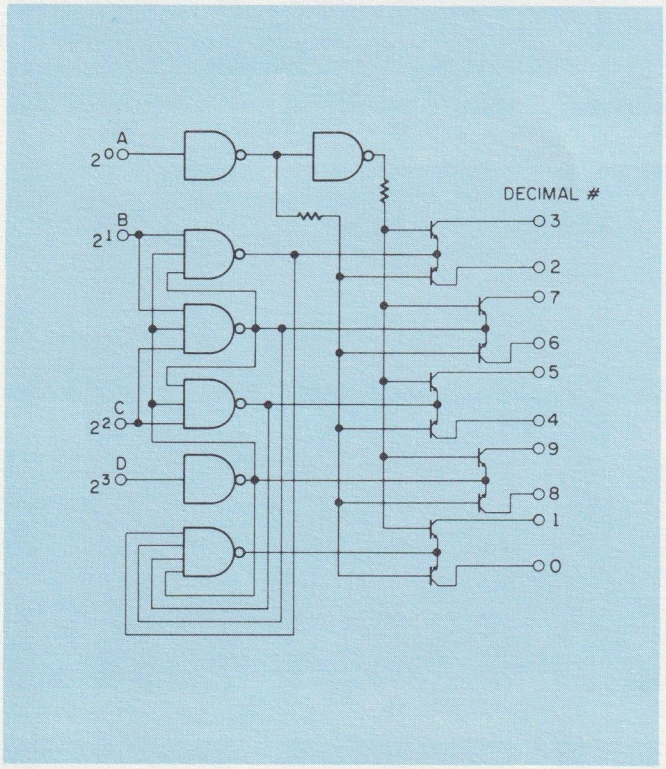

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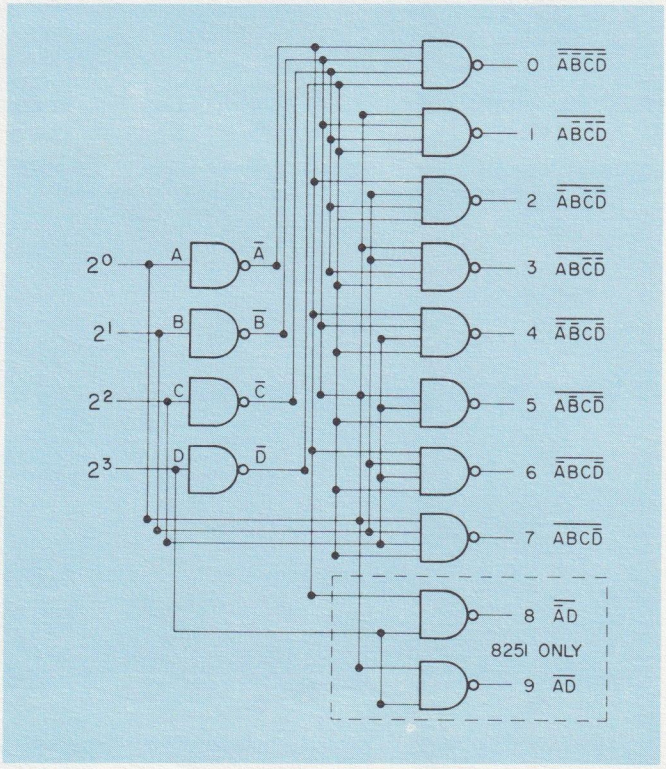

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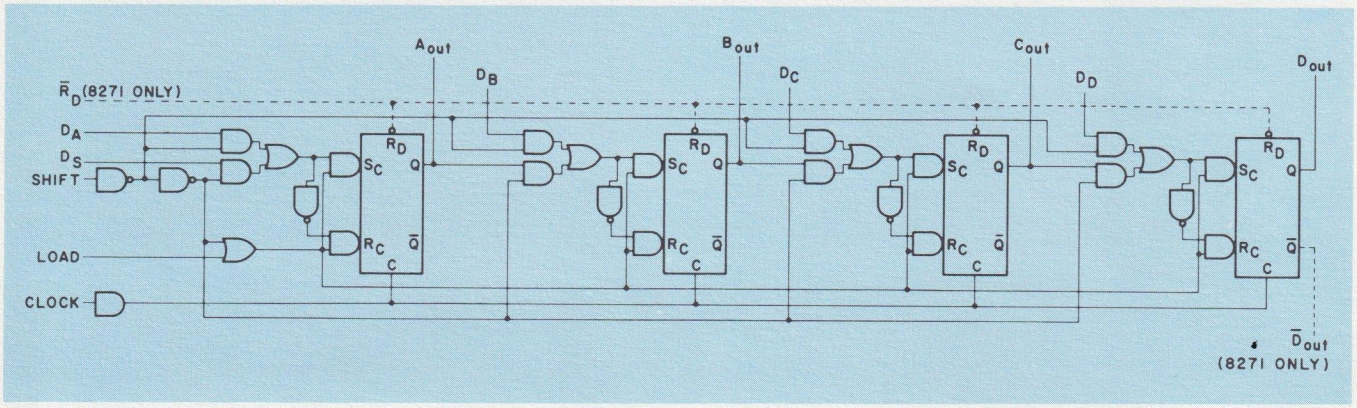

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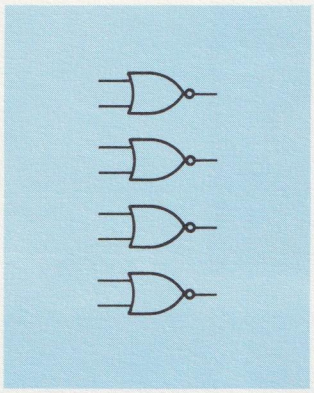

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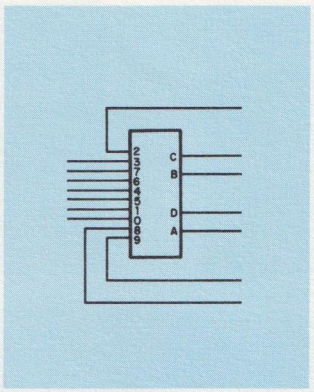

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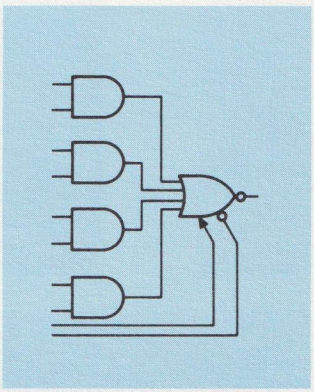

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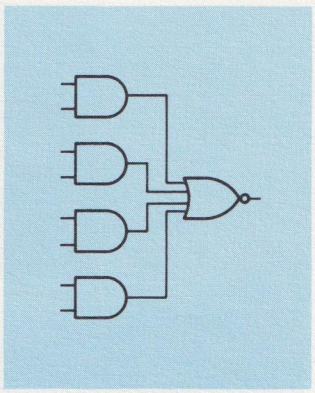

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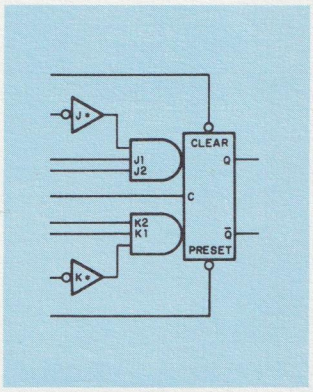

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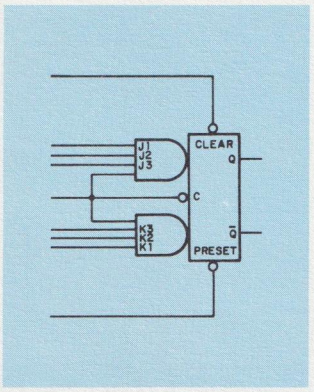

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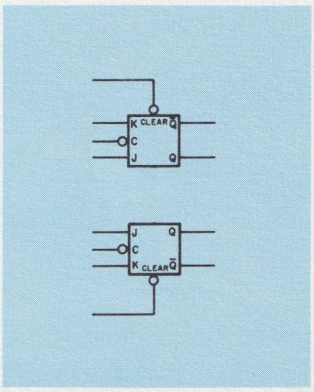

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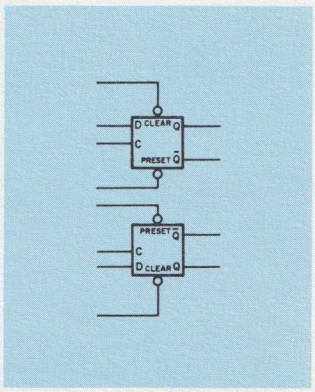

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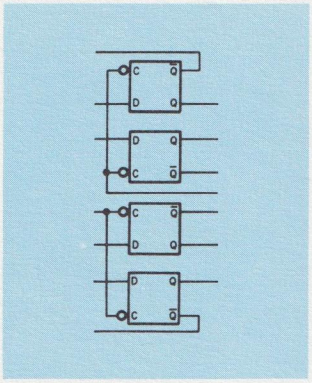

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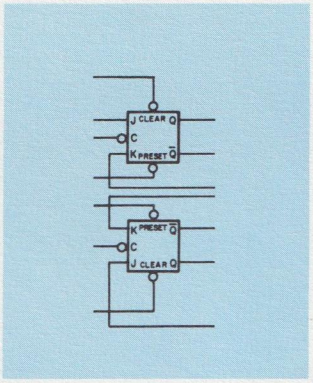

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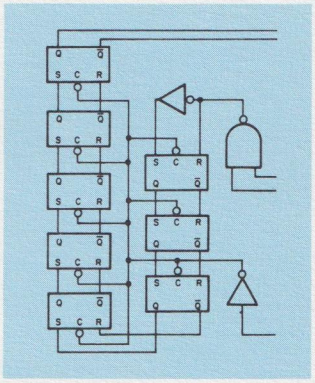

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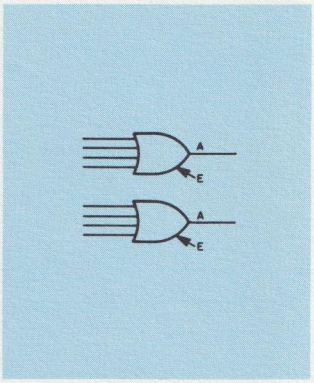

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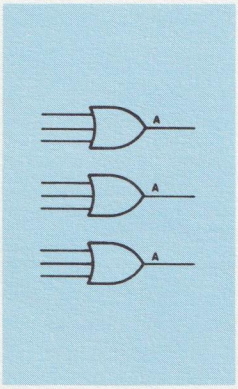

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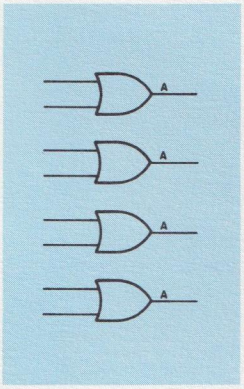

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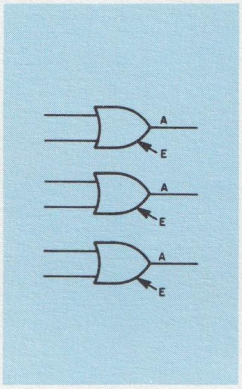

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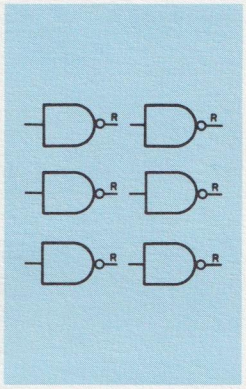

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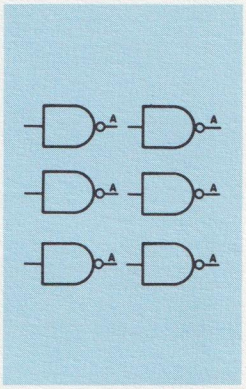

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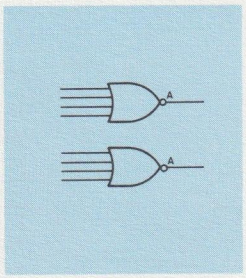
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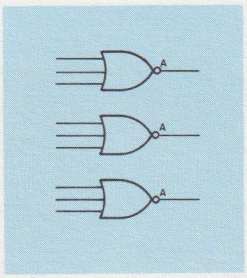
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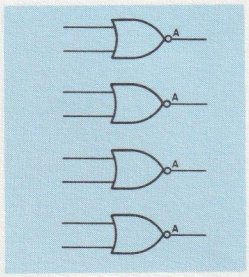
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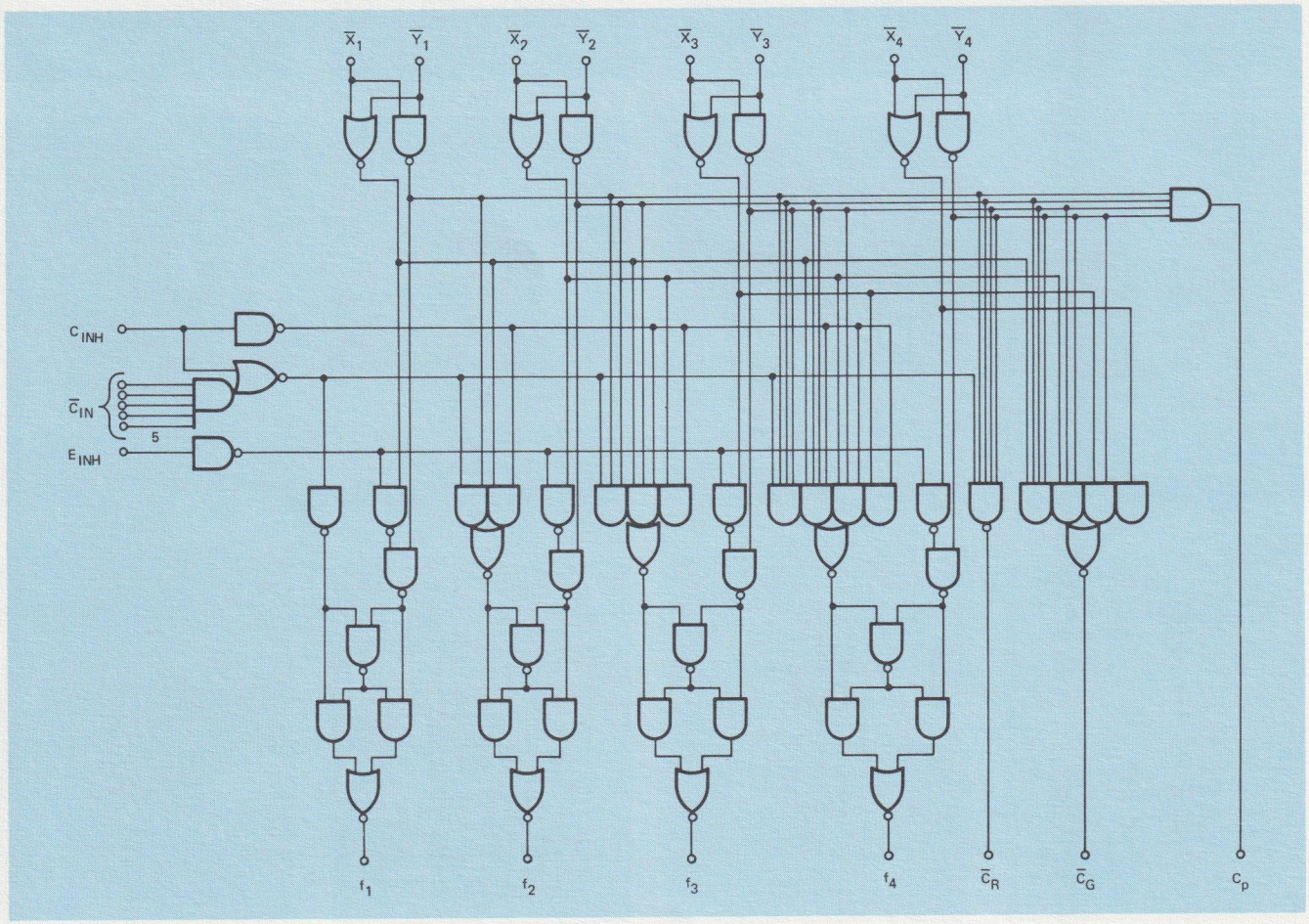
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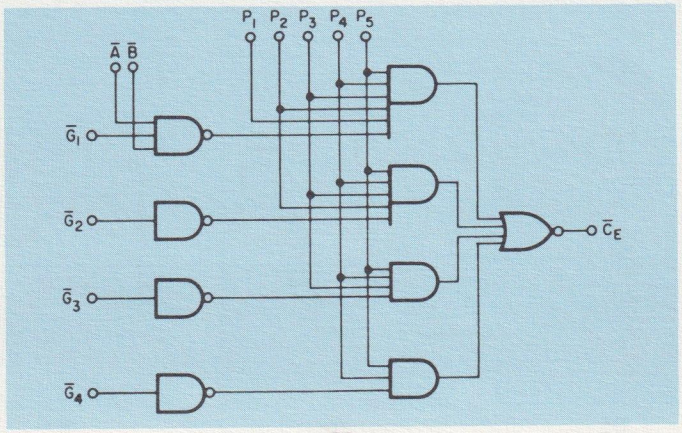
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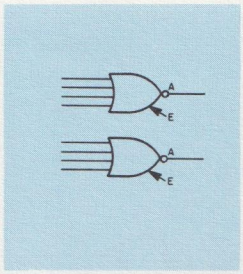

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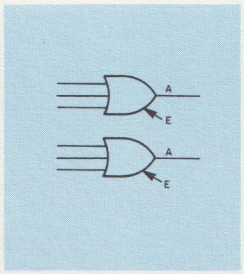

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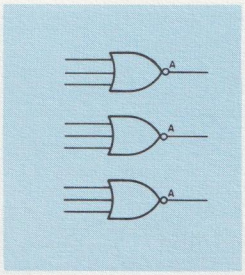

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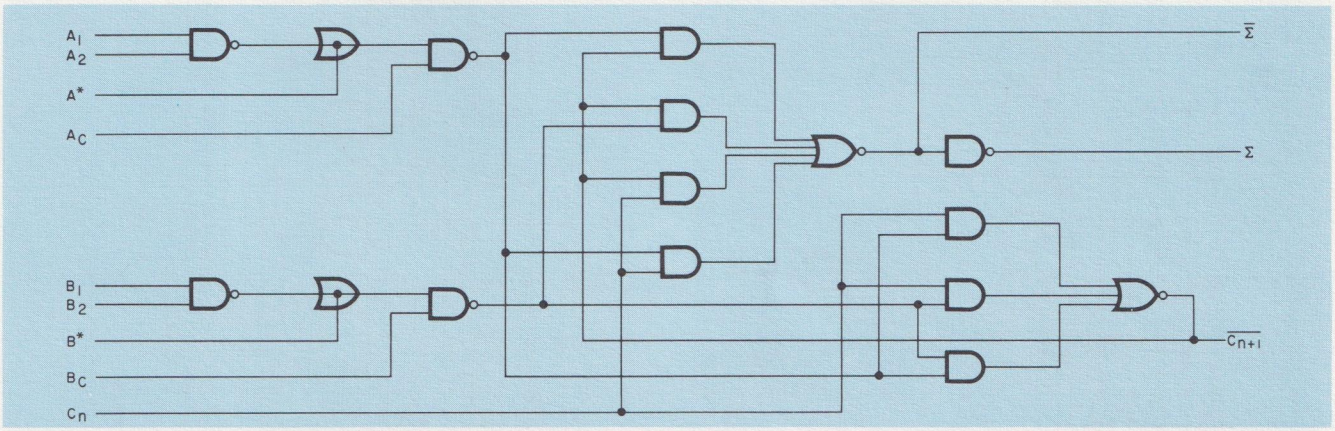

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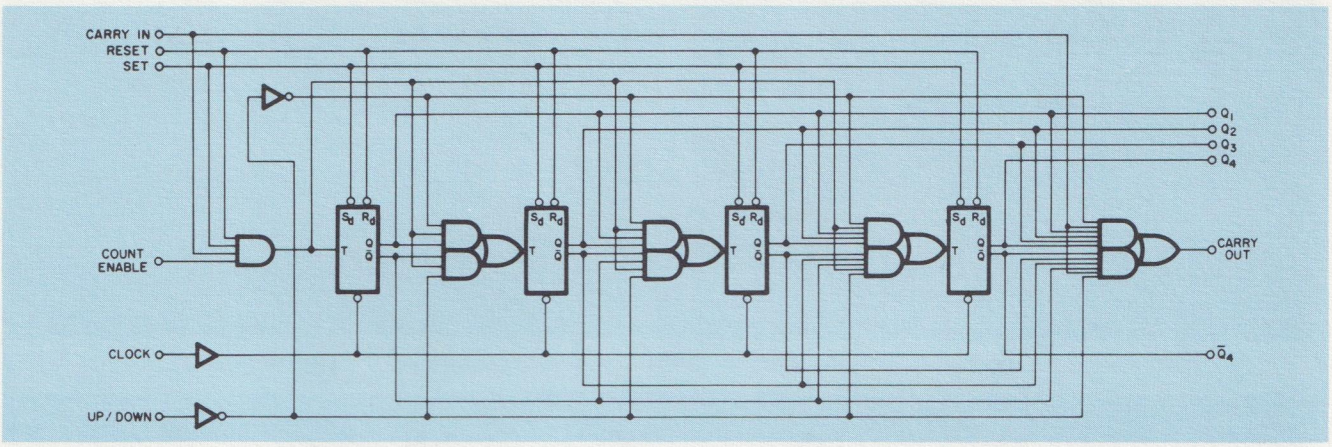

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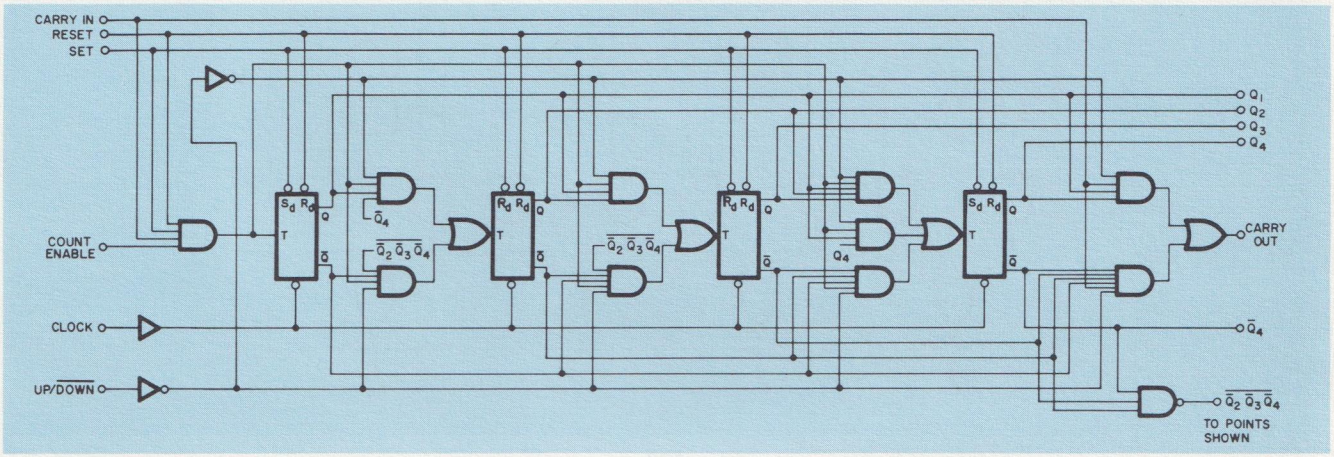

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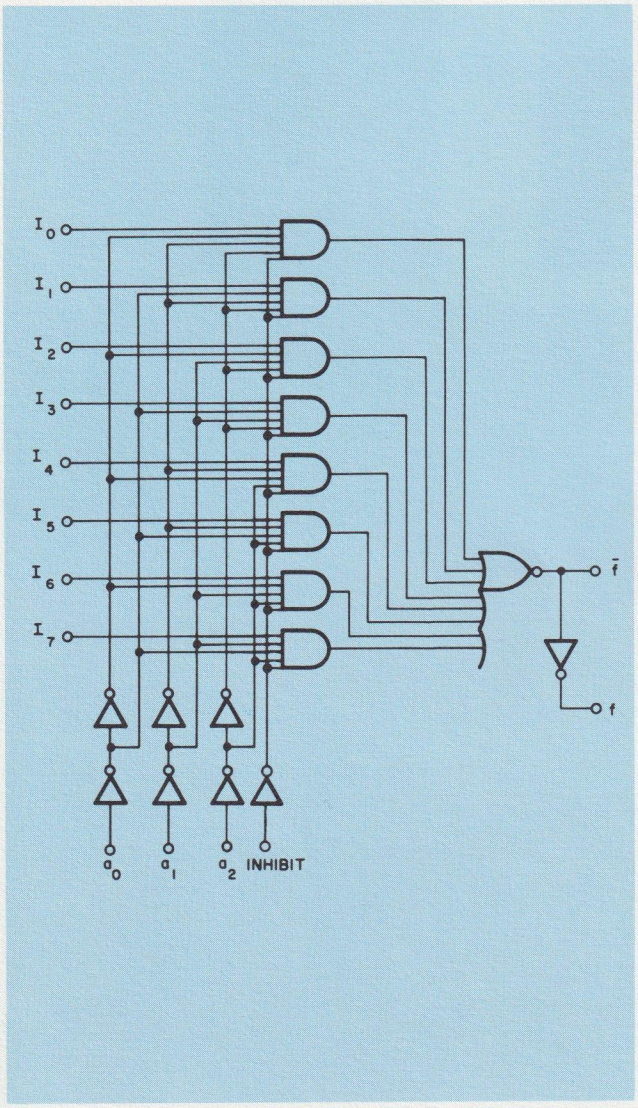
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I4
I5
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f
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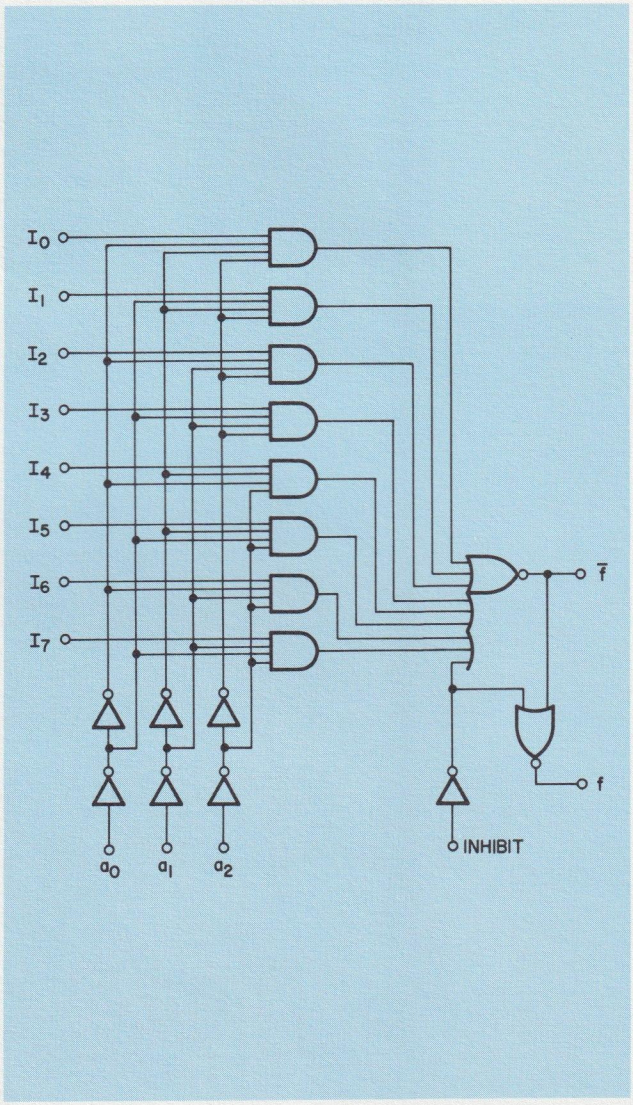
a1
a2
INHIBIT

100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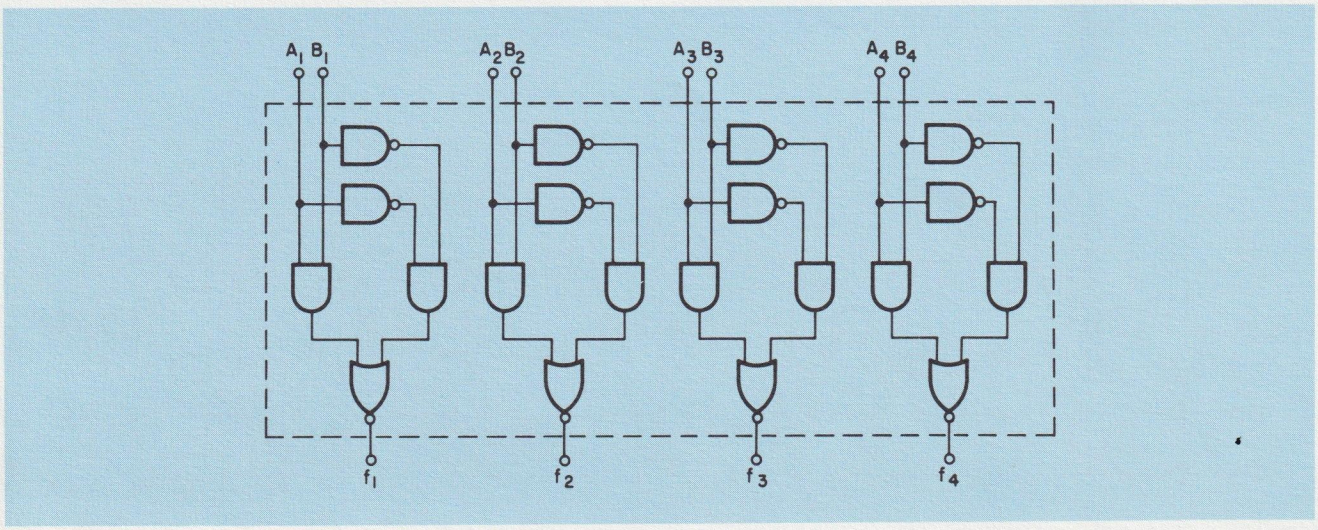
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f2
f3
f4

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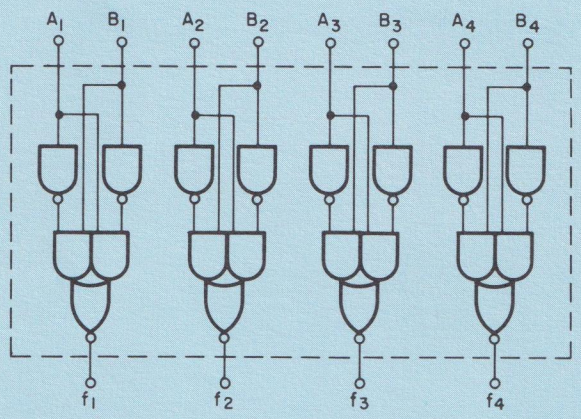
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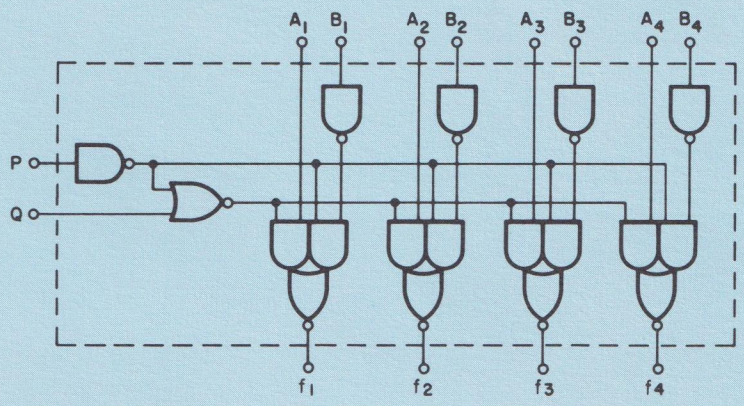
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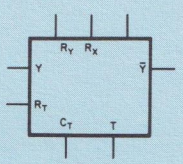
P
Q
f1 f2 f3 f4

104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105

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